HR-16/HR-16B Drum Machines Service Manual V1.00 7/27/95

PREFACE

This document is intended to assist the service technician in the operation, maintenance and repair of the HR-16 and HR-16B Drum Machines. Together with the HR-16/B Reference Manual, this document provides a complete description of the functionality and serviceability of these machines. Any comments or suggestions you may have pertaining to the document are welcome and encouraged.

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CAUTION

Danger of explosion if battery is incorrectly replaced.
Replace only with the same type or equivalent type recommended by the equipment manufacturer.

Battery Manufacturer: Tadiran

Type: TL-5101

Rating 3.6V

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- 1. <u>Power Source</u>. The product should only be connected to a power supply which is described either in the operating instructions or in markings on the product.
- 2. <u>Power Cord Protection</u>. AC power supply cords should be placed such that no one is likely to step on the cords and such that nothing will be placed on or against them.
- 3. <u>Grounding the Plug</u>. This product has a 3-wire grounding type of plug (a plug with a grounding pin) for safety purposes. This plug can only be used in a grounding power outlet. If the plug does not insert into the outlet you are using, the outlet probably is not a grounding type of power outlet. Contact your electrician to replace the obsolete outlet with a grounding type of outlet instead of defeating the safety feature of the grounding type of plug.
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- 5. Foreign Objects and Liquids. Take care not to allow liquids to spill or objects to fall into any openings of the product.
- 6. Water or Moisture. The product should not be used near any water or in moisture.
- 7. <u>Heat</u>. Do not place the product near heat sources such as stoves, heat registers, radiators or other heat producing equipment.
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 - b. The product is exposed to water or excessive moisture,
 - c. The AC power supply plug or cord is damaged,
 - d. The product shows an inappropriate change in performance or does not operate normally, or
 - e. The enclosure of the product has been damaged.

iv

General Troubleshooting

While this manual assumes that the reader has a fundamental understanding of electronics and basic troubleshooting techniques, a review of some of the techniques used by our staff may help.

- 1. Visual Inspection A short visual inspection of the unit under test will often yield results without the need of complex signal analysis (burnt, or loose components are a dead giveaway).
- 2. Self Test Alesis products that utilize microprocessor control contain built in test software which exercises many of the units' primary circuit functions. Self test should always be done following any repair to ensure basic functionality.
- 3. Environmental Testing Applying heat and cold (heat gun/freeze spray) will often reveal thermally intermittent components (Clock crystals, I.C.s, and capacitors are particularly prone to this type of failure).
- 4. Burn in Testing Leaving a unit running overnight often reveals intermittent failures such as capacitors that begin to leak excess current after a significant amount of time.
- 5. Cable Checks Wiggling cables can reveal intermittent failures such as loose cables or poorly soldered headers. Remember to check power supply cables as well.
- 6. Flexing the PC Board Poor solder joints and broken traces can often be found by pressing the PC Board in various places.
- 7. Tapping Componants Somtimes tapping on a component (particularly crystals) will cause it to fail.
- 8. Power Down/up Turning the unit off and back on rapidly several times may reveal odd reset and/or power supply failures.
- 9. Reset Threshold A Variac (variable transformer) can be used to check reset threshold levels. This can be particularly useful in helping customers with low line problems.
- 10. Compressors Using a compressor/limiter is often helpful when attempting to solve low level noise problems, as well as assisting with DAC adjustments.
- 11. Sweep Tests Sweep generators are very useful in checking the frequency response envelopes of antialiasing filters.
- 12. Piggybacking Piggybacking I.C.s is particularly useful when troubleshooting large sections of logic. This is especially true when working with older units.

TABLE OF CONTENTS

PREFACEii	ĺ
READ THIS!ii	ĺ
WARNINGSii	
SAFETY SUGGESTIONSi	V
General Troubleshootingv	
1.0 General Description	
1.1 Main PC Board Revisions1	
2.0 Power Supply	
2.1 Battery Backup2	,
2.2 PUP Circuit	,
3.0 The 8031	
3.1 Reset	
2.2 Mamory Mannad I/O	,
3.2 Memory Mapped I/O4	} 1
3.3 Keypad I/O	} •
3.4 MIDI I/O	
4.0 DM3AG ASIC	
4.1 Mask ROMs	
5.0 Analog Signal Paths6	
5.1 Drum Signal Output6	
5.2 Piezo/Data Slider Input6	;
5.3 Tape I/O6	;
5.4 Tape Output	7
5.5 Tape Input7	7
6.0 Test Procedures	7
6.1 General Testing	3
6.2 Internal Diagnostics and Hidden Keys	
6.3 DAC Adjustments	
7.0 Updates and Corrections	
7.1 New SRAM Supply Circuit	
7.2 Glass Zener (D15)	
7.3 Dirty Cliff jacks	
7.4 Ground CE	
7.5 RF resistor1	
7.6 10K MIDI Resistor (R5)	
7.7 MIDI Pullup	
7.8 RF Shields	
7.9 LCD Contrast Adjustments	
7.10 DAC Drift	
7.11 Old Keypad PC Boards1	
7.12 Lifting R411	
7.13 Reset Capacitor1	
7.14 Sram Capacitor1	
7.15 Tape Capacitors1	
7.16 RF chokes1	
7.17 AQ reset threshold1	
7.18 AQ R1161	
7.19 Volume Slider Wiring1	3
7.20 PUP Capacitor1	
8.0 Common Solutions	
9.0 Service Parts List	
10.0 Software History	
11.0 MIDI Implementation	
12.0 Service Manual History	
	ונ ממ

1.0 General Description

Diagram 1 provides a simplified block diagram to show major sub systems. Note that the schematic reference designations and pinouts used in this manual refer to the AQ revision of both the main PCB, and schematic.

1.1 Main PC Board Revisions

There are 3 major main PC Board revisions.

- A-This was the initial release. This board revision will require the most extensive updating of the three.
- CA-This version of the board was a 4 layer design. While offering several advantages over the older version (improved R.F. characteristics, smaller size, etc.) it was found to be extremely difficult to service (internal shorts can only be repaired using lifted pins and jumpers).
- AQ-This was the final revision. This revision will of course need the fewest updates, and should be relatively easy to troubleshoot.

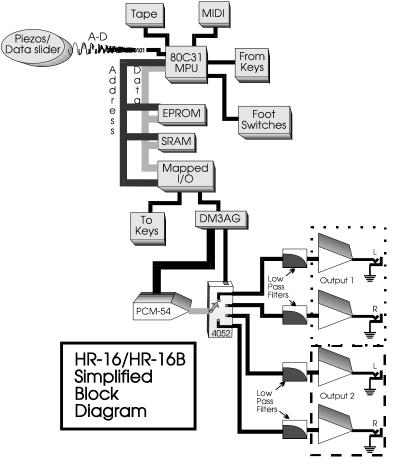


Diagram 1

Diagram 2 is provided in order to assist with board revision identification.

2.0 Power Supply

The power supply begins with the 9 Volt A.C., adapter (Alesis P2 [mini plug] or P3 [barrel] types). Input from J1 is R.F. filtered before on/off switch S1. From there it is split for the +12V, -12V, and +5V rails. The +12V rail consists of a voltage doubler (C1, C3, and D2, D3), a 7812 regulator (U8), and a filter capacitor (C6). The -12V rail is a "mirror" of the +12V rail, consisting of voltage doubler (C2, C4, and D1, D4), a 7912 regulator (U9), and a filter capacitor (C7). The +5V rail consists of a rectifier diode (D5), a filter capacitor (C5), a 7805 regulator (U10), and a multitude of $0.1\mu F$ bypass capacitors. Note that the raw +10V line used by the microprocessor reset, and the SRAM power supply (when retrofitted), is located at the input to the 7805 regulator. Note that revision AQ (the latest) boards also incorporate several R.F. suppression chokes and current limiting resistors. These have resulted in a few unique situations that may need to be dealt with (see section 7.16 for details)

2.1 Battery Backup

Battery backup is actually more complicated than it might first appear, as it depends on a good system reset (see section 3.1 for details) in order to function properly. The actual backup circuit consists of a battery (3V - 3.6V Lithium), a 10K resistor (R97) for checking standby current (see below), a "steering" diode (D7), a filter capacitor (C59), and a transistor/resistor/diode combination that acts as a steering diode. This combination may be missing on older board revisions, and must be installed (see section 7.1) to prevent data corruption due to a significant difference between V^{CC} and the amplitude of the data buss.

SRAM standby current should always be checked. While the unit is off, check the voltage across R97. If the voltage is higher than 80mV (specification, although a 1 to 20mV range is more normal) then a problem exists. Usually it indicates a bad (or simply wrong) SRAM, or a short somewhere along the MEM PWR line. Note that for a short time Sony 58256-PM (high power) SRAMs were being installed at the factory, causing batteries to drain in about 1 year. They should be replaced with low power versions (58256-LP) when found, in order to eliminate excess battery drain. We are currently using Hitachi 62256ALPs as replacements.

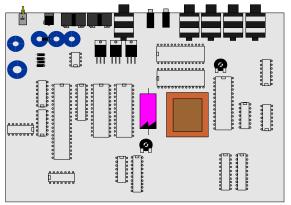
CAUTION: Danger of explosion if battery is incorrectly replaced. Replace only with the same type or equivalent type recommended by the equipment manufacturer.

Battery Manufacturer: Tadiran
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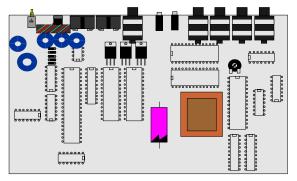
Rating 3.6V

2.2 PUP Circuit

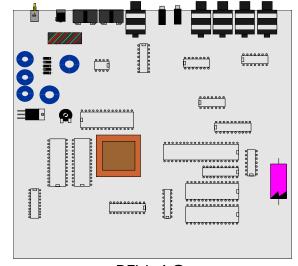
The PUP (quiet Power UP) circuit is designed to prevent the unit from making noise during power up. Note that this circuit will not be present on the earliest main PC boards. The circuit utilizes the RESET line (section 3.1) to control the power supply



12-22-87 (REV. A)



REV CA (Four Layer)



REV. AQ Diagram 2

lines to U20, which is the final active stage before the output jacks. Since both rails operate similarly, we'll only take the time to explain the operation of the + rail.

During power up, the RESET line is held low until the regulators are fully functioning. At this point, Q11 is turned off by RESET via R104. This has the affect of turning off Q10 by allowing the base of Q10 to pull high via R101. As soon as the reset line goes low, Q11 will turn on, pulling the base of Q10 lower. Q10 is now biased into saturation, allowing roughly +12V to be fed to the opamps. C65 is provided for extra filtering. The - rail consists of R99, R100, R105, Q12-Q13, and C64.

C62 was added to the analog rails of the op-amp to prevent oscillation during power up, and may need to be added to some older units (see section 7.20).

3.0 The 8031

The 8031 MPU is the heart of the HR-16's control section. It handles everything from keypad input and MIDI I/O, to sequencing. Note that the 8031 data buss serves a dual purpose. This buss multiplexes between low order addresses (1st 8 bits), and data. Latch U7 is used to hold the low order address half, during 8031 read and write cycles. The EPROM (U11) is used to hold 8031 program information. The SRAM (U12) holds system variables, as well as user sequence data. Z1 provides the 12MHz 8031 clock. MIDI I/O is handled through the 8031's built in RXD (Read Serial Data), and TXD (Transmit Serial Data) ports. Tape I/O and piezo input is handled through the built in 8031 I/O ports. DM3AG ASIC control, and LCD output are handled through memory mapped I/O (see section 3.2). Keypad decoding uses both forms of I/O (see section 3.3).

3.1 Reset

The 8031 reset circuit is perhaps the single most important circuit in the HR-16. When this circuit is functioning incorrectly, problems ranging from loss of battery backup to a complete lock-up of the machine can occur. A thorough knowledge of the operation of this circuit will greatly facilitate troubleshooting this unit.

This circuit uses the differential between raw +10V and regulated +5V to generate the required signals for system RESET. This is necessary due to fact that the system MUST be in a reset state while powering down, otherwise random noise on the 8031 data and address busses could corrupt SRAM data, and destroy any hope that the battery backup will work. R28, R29, and the 5.1V zener diode (D15) work together as a voltage divider to the base of Q4, and is designed so that transistor Q4 will turn on when the raw +10V supply is roughly 7V. This is to ensure that RESET does not occur until after the +5V regulator is fully functioning (i.e. +5V rail is solid). If RESET occurs too early, noise on the +5V rail can cause data corruption. Before the Q4 turn on threshold, Q5 remains turned on (the base of the transistor being pulled up by R30). This in turn holds the voltage across C20 at .3 volts. This is below the threshold (set by R25 and R96) necessary to turn on the comparator U1 (pins 10, 11 and 13), leaving the reset line high (pulled up by R10). Once the raw supply has reached a sufficient level to turn on Q4 (roughly 7V), Q4 will pull the base of Q5 low, turning it off. This allows C20 to begin charging through R24. Once C20 has charged to roughly 2.5V, the comparator will switch states and hold it low (due to the hysteresis established by R27). This completes the reset cycle during power up.

During power down, the opposite occurs, ensuring that the 8031 is held in a reset state during power down as well. This is necessary in order to prevent random data from being written into the SRAM during shutdown. Be aware that this can cause unusual unit lockups to occur if the circumstances are just right. For example, if an HR-16 was shut off while in record mode, it's possible the 8031 was put into reset in the middle of writing a two byte pointer into memory. If only one of those bytes is written before reset, then it may point to an incorrect location in memory (battery backup holds the incorrect data). When the unit is powered back up, the incorrect pointer may send the software into "never never land" where the only way to recover is to reinitialize the unit.

3.2 Memory Mapped I/O

In order to easily control the vast number of hardware functions that the 8031 needs to access, a system of memory mapped I/O is used. The basic idea is to make hardware functions appear to the 8031 as unused memory locations. That way all that the software has to do is write to a memory location in order to send that information to a specific device such as the LCD, or ASIC.

74HC138 (U13) performs the majority of the work in this circuit. Two things are required before U13 becomes active. 1> A15 must be low (i.e. the 8031 is accessing the lower 32K of address space). 2> The 8031 WRite line must be active (the 8031 is performing a memory write). A15 is used to directly control which function (memory or I/O) is active.

Once U13 is enabled, addresses A8-A10 are decoded by it, and the latch corresponding to the value of the decoded address is strobed. At this point, data on the 8031 data buss is "written" into the latch.

3.3 Keypad I/O

Keypad I/O is handled through a simple polling process Each row of the keypad matrix is pulled low one at a time (via U14 which is memory mapped). If any button along the row is pressed,

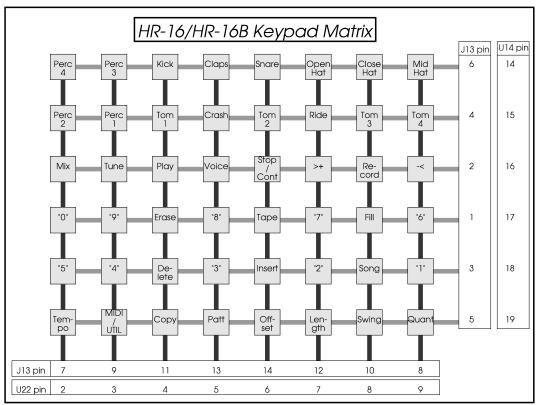


Diagram 3

the corresponding column input (U22) will high. lf appear buttons are pressed, all column inputs will appear as a low. D9-R42-R47 D15 and provide protection for the outputs of U14. Use diagram 3 to localize individual button failures.

3.4 MIDI I/O

The MIDI hardware is a standard implementation. MIDI out begins at the 8031's TXD port (pin 11) and travels via R6 to the darlington pair Q1/Q2. Note that the 8031's internal pullup is not very strong, and older units (revision A)

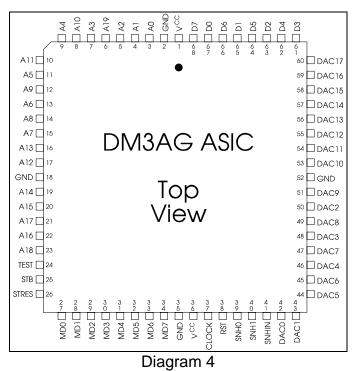
may require the addition of an external pullup resistor for the MIDI out to function correctly (see section 7.7).

MIDI in consists mostly of the opto isolator (U4), protection diode D6, pullup R7, and threshold resistor R5. Note that the threshold resistor may need to be changed in order to eliminate false MIDI triggers (see section 7.6).

4.0 DM3AG ASIC

The DM3AG ASIC is a complex LSI device, specifically designed for the purpose of playing percussion samples. Obviously, the internal workings of such a device are beyond the scope of this manual. However, a brief description of some of the important pins follows.

NAME	PIN#(s)	Function
MD0-MD7	27-34	8031 Data Buss Input.
CLOCK	37	Asic Clock Input (6MHz in HR-16).
DAC0-DAC16	42-51, 53-60	Output to DAC.
A0-A19	3-17, 19-23	Mask Address Buss
D0-D7	61-68	Mask Rom Data Buss
SNH0	39	Output Sample and Hold Control
SNH1	40	11 11 11 11
SNHIN	41	Output Sample and Hold Inhibit.
STRES	26	Instruction reset strobe.
STB	25	Instruction latch strobe.



67 9 61 63 65 1 3 5 7 VCC D0 Α2 D3 D2 D1 ΑO Α3 A4 60 66 2 11 10 68 4 6 62 64 DAC17 D4 D6 GND A10 A11 58 59 13 12 DM3AG DAC15DAC16 Α6 Α9 56 57 15 14 DAC13DAC14 Α7 Α8 ASIC 54 55 17 16 DAC11DAC12 A13 Socket 52 53 19 18 DAC10 GND A14 GND 50 51 21 20 DAC2 DAC9 A17 A15 49 23 48 22 DAC3 DAC8 A18 A16 47 25 46 24 DAC4 DAC7 STB TST 44 45 42 40 38 36 34 32 30 28 26 RST V^{CC} DAC5 DAC6 DAC0 SNH1 MD7 MD5 MD3 MD1 STRES 37 35 31 27 43 41 39 33 29 DAC1 SNHIN SNH0 CLOCK GND MD6 MD4 MD2 MD0

4.1 Mask ROMs

Diagram 5

The mask ROMs contain the all of the sample information. The 18 bit address buss allows for 2 megabytes per mask ROM. Address line A19 from the ASIC is actually used in conjunction with Q15 to switch the Mask ROM CE lines (pin 22) such that only one device is enabled at any given time.

5.0 Analog Signal Paths

5.1 Drum Signal Output

The output of the DM3AG ASIC is an 18 bit value. This may seem a little strange at first, since we are using a 16 bit DAC. R63 and R73-R75 provide the binary weighted resistor network necessary to achieve a full 18 bit output.

The PCM-54 DAC adjust circuit consists of R52, R53, R54, C34, and trimpot R90 (see section 6.3 regarding adjustment).

The output of the DAC is sent via R68 to the 4052 analog switch (U19), where the ASIC controls to which output (out1 left/right or out2 left/right) the final signal will be sent. (Note that stereo panning is achieved by sending the same signal to the left and right sides separately.)

Each output section (consisting of 1/4 of U20, 1/4 of U21, and misc. resistors and capacitors) serves the dual purposes of filtering and buffering (with a little gain added in). In the case of output 1, the signal is fed through the volume slider (via J11)(see section 7.19 regarding differences in wiring) before final output to the 1/4 inch jacks.

5.2 Piezo/Data Slider Input

Successive approximation is the method used to determine the value of the keypad piezo crystals (keypad velocity), and the data slider. It is a heuristic approach to the process of analog to digital conversion. The idea is to divide the process into short, manageable sections. Each significant binary weight (starting with the Most Significant Bit) is taken in turn, thus requiring only 8 comparisons to achieve a final value.

74HC04s U2 and U3 (replaced by a single 74HC540 [U2] in revision AQ PC boards) combine with the binary weighted resistor network (R16-R20, and SIP R22) to form a simple 8 bit digital to analog converter. The 8031 sends values to the DAC via it's internal I/O ports. The analog equivalent of these values is compared to the actual input signals via comparators U1 (pins 2, 4, and 5 for the data slider) and U1 (pins 8, 9, and 14 for the piezos). The 8031 reads the result of the comparison through I/O port P3.4 (pin 14) or port P3.5 (pin 15) and proceeds according to that result. The data slider is read directly via R23 (with C16 acting as a filter to reduce "jitter"). However the piezos require a little bit of wave shaping and translation before they can be read. First, the signal is A.C. coupled by C50, and rectified by D19. Q3 is then used to translate the signal into a 0V to 5V range (the piezos can produce up to about 50V). The signal is now ready for conversion.

5.3 Tape I/O

Tape output is very simple, while tape input is somewhat more complicated. This is due to the fact that tape backup and tape sync have different requirements. Data transfers need data integrity which implies guaranteed highs and lows, while tape sync needs tight timing and fast transistions. It's important to remember that not all tape decks are created equal. Probably the largest factor involved is the decks input and output capacitances. These can greatly affect the signals sent to and from the deck, and may cause some decks to be incompatible with the tape I/O needs of the HR-16. However, these cases should be rare, as the components chosen for the HR-16 are based on the industry "standards" that most manufacturers adhere to.

While we have heard many complaints regarding tape back up, we have actually found very few actual tape failures. Most of the complaints arise from user error, so below is a list of successful backup and tape sync strategies.

- 1. When attempting to save to a stereo cassette deck, use only the 1 channel (using both channels may result in odd phase cancellations during playback).
- 2. Avoid using any noise reduction systems (i.e. Dolby, or DBX) as these can distort the timing of the pulse train that contains the data.

- 3. Avoid using adapters for two reasons. 1> Some adapters contain built in attenuators that can result in extremely reduced levels, both to and from the tape. 2> Oxidation and "wear and tear" can cause adapters to become intermittent.
- 4. Always make several copies of each "save". It's especially smart to make copies on at least 2 different tapes as well. This reduces the chances that tape dropouts will cause loss of data.
- 5. Always use normal bias tapes, as high bias tapes actually end up recording noise, which could make it past the wave shaping circuitry and cause false triggers.
- 6. Always verify tapes after saving them. This helps reduce the chances of bad saves. Note however that the HR-16 does not compare the tape to the contents of memory. It simply verifies that the information on the tape is valid HR-16 data.
- 7. Experimentation with record and playback levels usually lead to better results.

Trouble shooting tape problems should begin with listening to the data tape audibly. This can help the technician determine if the problem occurs during tape save or load. If unusual dropouts are heard then the problem is either just a bad tape, bad cable, or the tape save circuit. Normal sounding tapes usually indicate a tape load problem. Only practice will help you determine what is "normal".

5.4 Tape Output

The tape output hardware is simply the 8031 output port P3.2 (pin 12), a pullup resistor (R40), and a voltage divider (R39 and R39) for achieving a line level output. The output during tape save or type sync out applications will appear as a .5V pulse train, but only if the tape out is NOT connected to a deck (the decks A.C. coupling will distort the output).

5.5 Tape Input

In it's simplest form the tape input consists of an integrator (under software control of the 8031) and a threshold detector (U1C). Input from J5 is passed through a current limiting resistor (R112) and on to the integrator (C11, C23, R86). The software controls the integration characteristics through Q16 via memory mapped I/O latch U14 (see section 3.2). While the unit is in 'TAPE SYNC IN' mode, U14/P12 is held high, turning on Q16 and sinking the majority of current through the integrator to ground. This provides for faster operation of the detection circuitry. D17 is used to prevent leakage of the integrator signals through the control circuitry during 'TAPE LOAD/VERIFY' operations (when U14/P12 is low).

The threshold detection circuitry surround U1C is relatively straight forward. R14 and R15 establish the threshold level with R12 and C9 acting as a filter to stabilize the threshold level and prevent oscillation. R21 establishes some hysteresis and R13 is a pullup for the open collector output of the LM339. The output of the '339 is sent directly to the 8031 in the form of an interrupt line. Forcing the 8031 to respond immediately to tape input is necessary due to the timing constraints required for I/O (especially in tape sync situations).

6.0 Test Procedures

If possible, user data should always be saved (DataDisk, or equivalent, recommended) prior to servicing. While this may not be immediately possible (or possible at all), it should be attempted as soon as possible.

6.1 General Testing

General testing should, at a minimum, consist of self test, and a short audio test (including testing key response and recording and playing back a pattern). More extensive testing would include:

- Checking battery backup
- Actually sending and receiving MIDI information
- Saving and loading data from tape
- Copying full patterns to themselves, then to other patterns so that memory becomes completely full (this ensures that the 8031 address buss functions correctly, as the self test does not take addressing into consideration).

6.2 Internal Diagnostics and Hidden Keys

Below is a list of the key presses necessary to activate hidden functions.

Power up while holding "ERASE", "DELETE", and "RECORD"Clear memory/Reinitialize system.
Power up while holding "QUANT" and "MIDI UTIL"Self test.
Hold "PATT" and press "VOICE"to exit).

Be aware that the self test will erase all internal memory (equivalent to reinitializing).

To perform the internal diagnostics, connect a MIDI cable between MIDI in and out. Connect a 1/8 inch cable between Tape in and out. Activate the self test (keys above). the order of items tested is:

1 ROM Test	Tests EPROM for errors
2 RAM Test	Tests SRAM for errors

3 MIDI I/O Test Tests MIDI input/output functions 4 TAPE I/O Test Tests Tape input/output functions

5 LED Test Lights each front panel LED for a couple seconds 6 DAC Adjust Enters DAC adjust mode (press stop to exit).

6.3 DAC Adjustments

The only adjustment necessary in the HR-16 is the DAC adjustment. This is normally done at the end of the HR-16's internal diagnostics, however holding the "PATT" button and pressing the "VOICE" button simultaneously also starts the DAC adjust routine. While this routine is running, adjust R90 (the trimpot near the PCM-54 DAC) so that a minimum of noise is heard during each drum hit. A DAC that is out of adjustment will "buzz", particularly at the end of the sample. Note that you may have to turn your amplifier up in order to hear this signal. Once the adjustment is complete, hitting the "STOP" button ends the DAC adjust routine.

7.0 Updates and Corrections

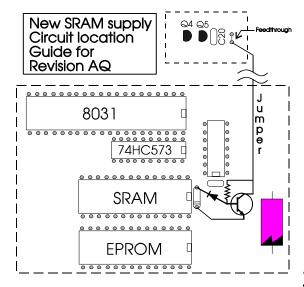
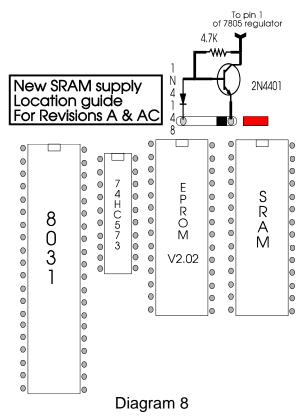


Diagram 6



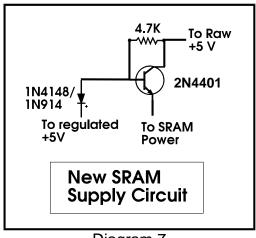


Diagram 7

7.1 New SRAM Supply Circuit

• All Revisions.

The new SRAM supply circuit (See diagram 7) supplies a solid 5V to the SRAM, preventing input data from being higher in amplitude than the supply voltage, which can cause data corruption. First, remove the original diode (D8), then install the new circuit. Diagram 8 shows the location to install the circuit in Revision A & CA PC boards, while diagram 6 shows the location for revision AQ PC boards. The installation of this circuit is highly recommended, and is absolutely necessary if a 58257 SRAM is in the unit. This is because '257s are much more sensitive to supply voltage the older '256 SRAMs.

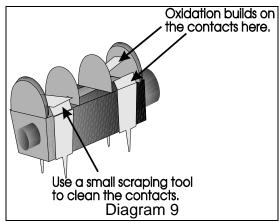
7.2 Glass Zener (D15)

Revisions A & CA.

For a short time, glass package 1N5231B zener diodes were used instead of the more familiar metal package. These were found to be unreliable, and should be replaced with metal package zeners.

7.3 Dirty Cliff jacks

All Revisions.

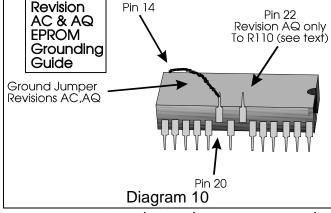


Occasionally, oxidation will build up on the cliff jack contacts, causing the jack normaling to fail. When this happens, some drum sounds will be "lost" when using the unit in mono. (Only one cable plugged in). The solution is to thoroughly clean the normaling contacts (See diagram 9 for location).

7.4 Ground CE

All Revisions.

It was discovered that many units returned for odd crashes all appeared to have a common component (National EPROMs). After further investigation it was revealed that it was not due



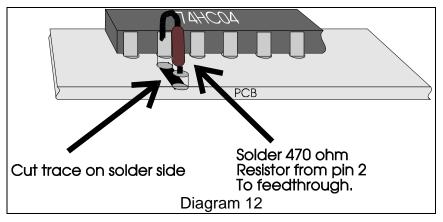
. G . . r 0 . u n 0: _{Cut} d 0 İ n g CE Solder Side 0 **SRAM** n R 0 0 е 0 0. 0 0 S 0 n .0 Diagram 11

defective components. but due to minor to "incompatibility". It was determined that using CE (pin 20) to enable the device took too long, and the 8031 would occasionally attempt to read it's instructions before the data was valid. The solution to this effect was to leave the EPROM permanently enabled, and use OE (pin 22), which operates much faster, to control it's access to the data buss. On revision A PC boards, this requires cutting a trace, scraping the solder mask from the closest ground trace and adding a jumper (see diagram 11). On revision CA PC boards, this requires that pin 20 of the EPROM be lifted out of the socket, and a jumper installed (see diagram 10). On revision AQ PC boards, pin 22 of the EPROM must also be lifted, the end (away from the 8031) of R110 is lifted, and a iumper between the two is added. While non National exhibit this **EPROMs** do not seem scenario. recommended that this update be performed on all units.

7.5 RF resistor

Revision A.

An improvement of R.F. characteristics can be achieved by installing a 470Ω into the ASIC clock line. The best location to accomplish this is between the 74HC04 (U6) and the nearby feed through. The trace on the solder side of the PC board can then be cut (see diagram 12 for details).



7.6 10K MIDI Resistor (R5)

All Revisions.

Since the HR-16 was released, we have found that a 10K resistor provides a better signal threshold level to the opto isolator than the original 47K specified in the design. If the older value of 47K is found, then a 12K or 13K resistor soldered in parallel with R5 will achieve the desired threshold level.

7.7 MIDI Pullup

Revision A.

Some early units were prone to sending false or incorrect data through the MIDI out. This was traced to insufficient pull up resistance in the 8031's TXD port. This can be solved by installing a 4.7K resistor between R6 and R7 as shown in diagram 13.

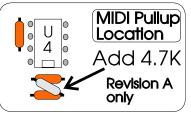
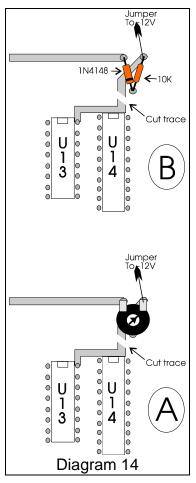


Diagram 13

7.8 RF Shields

Revision A.

In an effort to further reduce the R.F. emissions of the HR-16, a self sticking R.F. shield was introduced. Care should be taken when installing the shield, as wrinkles in the shield may easily



cause shorts to the main PC board. The tab of the shield should make a firm mechanical contact to ground when the board is in place (for a short time revision CA main PC boards were manufactured with the solder mask covering the ground plane that will need to be scraped off in order to achieve a proper connection) If this is not done correctly, this may actually create more R.F. noise than before (the shield starts acting as a capacitivly coupled antenna). Also note that some PC board revisions have the DAC adjust trimpot on the bottom of the board for external access. On these units, either cutting a out a circle around the trimpot, or the addition of electrical tape will insulate the trimpot from the shield.

7.9 LCD Contrast Adjustments

All Revisions.

Normally the LCD contrast is adjusted at the factory. However, in the event an older LCD is replaced, or the contrast is not enough to suit the user, it may be necessary to change the hardware to achieve a suitable contrast level. Diagram 14A shows the changes needed to convert older revisions so that the trimpot will function in a more appropriate range. Diagram 14B shows the latest configuration used on older revisions to achieve a nominal contrast level. In revision AQ boards, the only way to change contrast is by adding (or removing, if one is present) a jumper across D21 (located by J12).

7.10 DAC Drift

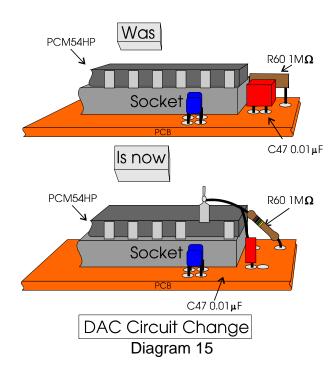
All Revisions.

It has been found that some PCM-54's linearity tend to drift with time and temperature. In order to improve the linearity 1 leg of R60, one leg of C47, and pin 27 of the PCM-54 should be lifted and soldered together (see diagram 15). This should only be necessary if the user complains of noise after the unit warms up.

7.11 Old Keypad PC Boards

Revision A

The original HR-16 came with standard PCB type contacts (tinned copper traces), but these were found to oxidize over time. This was especially evident when the unit was used in a moisture rich environment (such as near the ocean). We have since switched to using PC Boards with carbon contacts. We recommend replacing the older type PC Boards with the newer



variety. In the event that the newer board is unavailable (emergency rushes, etc.) it is possible to clean the old keypad contacts with a pencil eraser. While this will restore operation to the unit, such a measure is strictly temporary, as the contacts will eventually reoxidize.

7.12 Lifting R41

Revision A

It was found that the feed through below R41 (located near the battery) would occasionally short directly to the resistor above it. If this happens then battery backup will not function. The simplest solution is to lift one or both leads of the resistor slightly with a soldering iron (pushing them up through from the bottom of the board is probably the easiest). This should prevent any physical contact of the resistor to the feed through.

7.13 Reset Capacitor

Revision A & CA

The blue monolithic block RAM capacitors used throughout the board were found to be unreliable when used in timing critical applications due to excess leakage current. C20 is a prime example of just such an application. If C20 leaks too much, it acts as a voltage divider with R24, and never exceeds the threshold voltage required to finish the reset process. A large percentage of "locked up" units can be repaired by replacing this capacitor with either a ceramic disk or film (WIMA) type of capacitor. This replacement is recommended regardless of whether the capacitor seems to be failing or not.

7.14 Sram Capacitor

Revision A

The blue monolithic block RAM capacitors used throughout the board were found to be unreliable when used in timing critical applications due to excess leakage current. In this case the capacitor causes excess battery drain, and is the primary cause of battery failure. These capacitors should be replaced with either a ceramic disk or film (WIMA) type of capacitor, regardless of whether the capacitor seems to be failing or not.

7.15 Tape Capacitors

Revision A & CA

The blue monolithic block RAM capacitors used throughout the board were found to be unreliable when used in timing critical applications due to excess leakage current. Here, the capacitors reside in the tape input path (C11 and C23), and may cause the distortion of incoming tape signals. Such distortions can cause the loss of tape loading capabilities. These capacitors should be replaced with either a ceramic disk or film (WIMA) type of capacitor if tape loading failures occur.

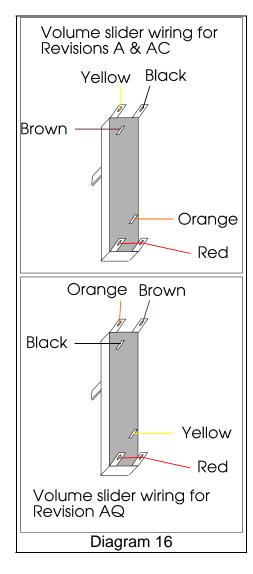
7.16 RF chokes

Revision CA & AQ

Occasionally the R.F. chokes on these board revisions (located near the power input jacks) will bust a lead during shipping. When this occurs, it may not be possible to repair the choke. In this case it is O.K. to remove the choke and add jumpers across its old location. In most cases this shouldn't be necessary as the units should have had their chokes hot glued to the board at the factory. Any units that have loose chokes need to be glued (hot glue recommended) to prevent future damage.

7.17 AQ reset threshold

Revision AQ



During the development of the AQ main PC board, one of the prime considerations was to reduce R.F. emissions to virtually 0. Towards this end, a 100 ohm resistor (R133) was introduced between the raw supply voltage and the rest of the circuitry to reduce power supply noise. This had the effect of increasing the threshold of the RESET circuit, and was found to cause some units to reset repeatedly in low power situations (i.e. use of lots of lights in a club could cause fluctuation in the local power by 15V to 20V, causing the unit to reset over and over again). R28 is part of the threshold circuit for the RESET line. Originally valued at 3K, the new value is 1.5K (easily obtained by adding an additional 3K in parallel). This will bring the threshold into a more reasonable range.

7.18 AQ R116

Revision AQ

Again an attempt to reduce power supply noise, this resistor was found to sometimes reduce the power supply level to the 8031 (and surrounding circuitry) to below the required 4.75V. It is recommended that a jumper be soldered across this resistor (located between the 8031 and U6).

7.19 Volume Slider Wiring

Note that the wiring of the volume slider changed between Revisions CA and AQ. Diagram 16 shows the correct wiring for each board style.

7.20 PUP Capacitor

Revision CA

When the PUP circuit first appeared, it was found that the circuit would occasionally oscillate on power up, causing noise. This was eliminated by adding a bypass capacitor (later incorporated as C62) across the power supply pins of U20 (pins 4 and 11).

8.0 Common Solutions

A thorough knowledge of the software history can help solve a great many situations quickly. Also be aware that with devices as full of options as the HR-16(B), there are even more possibilities for user error (i.e. the user claims that MIDI out isn't working, but on checking the settings, the tech finds that both MIDI clock, and DRUM NOTES OUT are turned off). Understanding how the user has the unit in his (her) setup is an important tool in troubleshooting units that act like there is nothing wrong with them.

While it is simply beyond the scope of this manual to present every possibility, the chart below offers a majority of solutions to common situations.

Complaint	Possible Cause	Solutions
Unit is truly "dead". (No lights, or sound)	Blown power supply.	Replace and retest.
	+5V rectifier blown (D5). (Note that 1N4001s were used originally, but some were found to be unreliable. We have since switched to using 1N4004s exclusively.)	Troubleshoot and repair as necessary.
	Blown DM3AG ASIC. (occasionally these devices will "short" and pull down the 5V supply rail)	Remove ASIC and attempt power up. Also note that this type of ASIC failure usually causes the ASIC to become extremely hot to the touch.
	Blown +5V filter capacitor (C5) Usually blown capacitors will display a "distended" appearance.	Troubleshoot and repair as necessary.
	Faulty or broken power jack.	Troubleshoot and repair as necessary.
	Faulty or broken power switch.	Troubleshoot and repair as necessary.
	Broken lead on power choke.	Troubleshoot and repair as necessary. (see section 7.16)
	Blown monolithic filter capacitor. (Any of the small blue RAM capacitors used as bypass capacitors can become shorted and pull the rail low. We are currently using ceramic disk capacitors as replacements exclusively)	Troubleshoot and repair as necessary. Note that when these capacitors fail, they often turn brown from overheating, and some will occasionally just burn up.
Unit powers up, but does not function. (No LCD display, all LEDs on, buttons don't work, etc.)	Unit is simply "crashed".	Reinitialize memory and test.
	C-20 leaking excessively.	Troubleshoot and repair as necessary. (see section 7.13)
	Faulty 8031, EPROM, or SRAM.	Troubleshoot and repair as necessary. (see section 3.X)
	Faulty DM3AG ASIC. (Pulling down the 8031 data buss.)	Troubleshoot and repair as necessary.
	Faulty I/O latch pulling down lines on data buss.	Troubleshoot and repair as necessary. (see section 3.2)
	Other faulty reset component.	Troubleshoot and repair as necessary. (see section 3.1)
	Open or short in 8031 data buss.	Troubleshoot and repair as necessary. (see section 3.X)
	Open or short in 8031 address buss.	Troubleshoot and repair as necessary. (see section 3.X)
	Faulty LCD pulling down lines on data buss.	Test with new LCD.
LCD shows no, or scrambled display (the rest of the unit seems to function normally).	Faulty LCD.	Test with new LCD.
,	Faulty LCD cable.	Replace and retest.
	Faulty 74HC138 (U13), or open between U13 and LCD header.	Troubleshoot and repair as necessary.
Intermittent reset.	C-20 leaking excessively.	Troubleshoot and repair as necessary. (see section 7.13)
	Faulty 8031, EPROM, or SRAM.	Troubleshoot and repair as necessary. (see section 3.X)
	D15 is glass package type (Revision A or CA only).	Replace with metal package type (see section 7.2).
	R116 is pulling 8031 V ^{CC} too low (revision AQ only).	Add jumper across resistor.
Complaint	Possible Cause	Solutions

(No battery backup. Battery is not dead.) Drum pads not sensitive to velocity. Unit "crashes" constantly. Complaint Unit "crashes" constantly. (cont.)	Faulty SRAM. Broken Piezo lead. Faulty cable. Faulty ADC circuit. Faulty reset circuit. Faulty 8031, EPROM, or SRAM. Open or short in address or data busses. Faulty DM3AG ASIC pulling down data buss. Possible Cause Faulty I/O latch pulling down data buss.	Replace and retest. Troubleshoot and replace as necessary. Replace and retest. Troubleshoot and repair as necessary. Troubleshoot and repair as necessary. Troubleshoot and repair as necessary. Solutions Troubleshoot and repair as necessary.
Drum pads not sensitive to velocity. Unit "crashes" constantly.	Broken Piezo lead. Faulty cable. Faulty ADC circuit. Faulty reset circuit. Faulty 8031, EPROM, or SRAM. Open or short in address or data busses. Faulty DM3AG ASIC pulling down data buss.	Troubleshoot and replace as necessary. Replace and retest. Troubleshoot and repair as necessary. Troubleshoot and repair as necessary. Troubleshoot and repair as necessary.
Drum pads not sensitive to velocity.	Broken Piezo lead. Faulty cable. Faulty ADC circuit. Faulty reset circuit. Faulty 8031, EPROM, or SRAM. Open or short in address or data busses.	Troubleshoot and replace as necessary. Replace and retest. Troubleshoot and repair as necessary. Troubleshoot and repair as necessary.
Drum pads not sensitive to velocity.	Broken Piezo lead. Faulty cable. Faulty ADC circuit. Faulty reset circuit. Faulty 8031, EPROM, or SRAM.	Troubleshoot and replace as necessary. Replace and retest. Troubleshoot and repair as necessary. Troubleshoot and repair as necessary.
Drum pads not sensitive to velocity.	Broken Piezo lead. Faulty cable. Faulty ADC circuit. Faulty reset circuit.	Troubleshoot and replace as necessary. Replace and retest. Troubleshoot and repair as necessary.
	Broken Piezo lead. Faulty cable.	Troubleshoot and replace as necessary. Replace and retest.
	Broken Piezo lead.	Troubleshoot and replace as necessary.
(No battery backup. Battery is not dead.)		
Not retaining memory when power removed.	power down).	Troubleshoot and repair as necessary.
Not retaining memory when power removed.	Faulty reset circuit (not going into reset during	current (see section 2.1). Troubleshoot and repair as necessary.
	(CE pin 20 not held high). Faulty battery.	Replace capacitor and battery. Check batte
	SRAM not in standby mode while power off	Troubleshoot and repair as necessary.
· · · · · · · · · · · · · · · · · · ·	Faulty or incorrect SRAM.	See section 2.1.
(No battery backup. Battery is dead.)	monoblock type).	current (see section 2.1).
Not retaining memory when power removed.	Faulty 8031. Faulty SRAM bypass capacitor (blue	Replace and retest. Replace capacitor and battery. Check batter
Foot switches not working.	Broken cliff (1/4") jack.	Troubleshoot and repair as necessary. Replace and retest.
	in the binary weighted resistor network).	section 5.2)
Data slider skipping numbers.	Faulty ADC circuit. (most likely a short or open	Troubleshoot and repair as necessary. (s
	the keypad velocity will not work either.) Faulty 8031.	section 5.2) Replace and retest.
	Faulty ADC circuit. (Usually if this is the case,	Troubleshoot and repair as necessary. (s
	board.	
Data slider not working at all.	Broken wire between slider and keypad PC	nepiace and relest.
Data slider not working at all	Faulty comparator (U1). Faulty slide potentiometer.	Troubleshoot and repair as necessary. Replace and retest.
	Faulty integrator capacitor (C11 or C23).	Replace and retest.
	Faulty 8031.	Troubleshoot and repair as necessary.
•	User error.	See section 5.3.
No tape in.	Broken 1/8" jack (J5).	Replace and retest.
	User error. Faulty 8031.	See section 5.3. Troubleshoot and repair as necessary.
No tape out.	Broken 1/8" jack (J6).	Replace and retest.
No ton a suit	Faulty 8031.	Troubleshoot and repair as necessary.
	Threshold resistor (R5) wrong value.	See section 7.6.
No (or intermittent) MIDI in.	Faulty opto-isolator (U4).	Replace and retest.
	Faulty 8031.	Troubleshoot and repair as necessary.
No (or intermittent) MIDI out.	Needs MIDI pullup resistor. Faulty Transistor (Q1 or Q2).	Add if necessary (see section 7.7). Troubleshoot and repair as necessary.
No (or intermittent) MIDL out	Faulty ribbon cable.	Replace and retest.
		cleaner (such as Blue Shower).
	Dirty rubber keypad.	Clean keypad contacts with non-resid
Intermittent buttons.	Old keypad PC Board.	Replace with new style keypad PC board a retest.
	actually fairly rare, but it can happen).	section 3.3)
	Component failure in keypad circuitry. (This is	Troubleshoot and repair as necessary. (s
	Faulty op-amp (U20, U21) or component in surrounding circuitry.	Troubleshoot and repair as necessary.
	Faulty Analog switch.	Troubleshoot and repair as necessary.
	default drum kit).	
	hard left or right (TOM 1 and TOM 3 of the	350001 <i>1.3)</i>
	Dirty, or broken cliff (1/4") jack. This is particularly noticeable on drums that panned	Troubleshoot and repair as necessary. (s section 7.3)
	default drum kit).	<u></u>
	hard left or right (TOM 1 and TOM 3 of the	
	outputs, volumes set to)etc.). This is particularly noticeable on drums that panned	necessary.
No sound from a particular drum.	User error (i.e. drum pads set to wrong	Check operating parameters. Adjust them
	outputs, volumes set to)etc.).	
	User error (i.e. drum pads set to wrong	Check operating parameters.
	analog switch, or op-amp. Faulty volume slider.	Test AUX outs. Repair as necessary.
No sound at all.	Faulty DM3AG ASIC, PCM-54 DAC, 4052	Troubleshoot and repair as necessary.
	Other faulty component is 8031 reset circuit.	Troubleshoot and repair as necessary.
	AQ only).	7.17).
ntermittent reset. (cont.)	R28 (reset threshold) is wrong value. (Revision	Add another 3K resistor in parallel (see section

Some or all drum sounds are distorted.	PCM-54 DAC out of adjustment.	Adjust according to section 6.3.
	Faulty PCM-54 DAC.	Replace and retest.
	Incorrect EPROM. (Oftentimes users will attempt to install the HR-16A/B EPROM into their new HR-16B. WRONG! This EPROM is intended to be used only in the HR-16, and does not have the correct MASK ROM addressing tables to play HR-16B sounds).	Check and replace if necessary.
	Faulty DM3AG ASIC.	Replace and retest.
	Faulty power supply rail.	Troubleshoot and repair as necessary.
	Faulty PUP circuit (one rail not making it to the op-amp).	Troubleshoot and repair as necessary.
Volume slider only works for 1/2 of it's range.	Slider wiring incorrect for particular main PC Board revision.	See section 7.19.

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9.0 Service Parts List

r						
GROUP	DESCRIPTION	PART#	QTY	POSITION	PCB	NOTES
ASY	PCB, D1 MAIN REV AQ	8-20-0038	1	REV: AQ		
ASY	PCB, D1 KEYPAD	8-20-0040	1			
ASY	CASE TOP ASSY D1	8-20-0009	1			
ASY	CASE TOP ASSY D2	8-20-0010	1			
CAB	14 PIN DIL 7	4-18-0714	3			
CAB	5 PIN SIL 5	4-19-0505	1			
CAP	0.1 MFD CERDISC	1-02-0104	23	C11,23,60,61,66-71,73-83,73,80	MAIN	
CAP	2200 MFD ELEC	1-08-2200	1	C5	MAIN	
CAP	330 MFD ELEC	1-09-0337	3	C1-3	MAIN	
CAP	470 MFD ELEC	1-09-0477	1	C4	MAIN	
CAP	4.7 MFD ELEC	1-12-0475	7	C6-9,22,64,65	MAIN	
CER	100 PFD CERDISC	1-02-0101	1	C63	MAIN	
CER	150 PFD CERDISC	1-02-0151	11	C71,84-90,92-94	MAIN	
CER	27 PFD CERDISC	1-02-0270	2	C18,19	MAIN	
CON	14 PIN DIL HDR	4-14-0014	5	J12-14, (2 ON KPD PCB)		
CON	5 PIN SIL HDR	4-15-0005	1	J11	MAIN	
FIL	1000 PFD FILM	1-20-0102	7	C16,31,37,48,49,57,58	MAIN	
FIL	0.01 MFD FILM	1-20-0103	4	C34,50,60,62	MAIN	
FIL	0.1 MFD FILM	1-20-0104	3	C17,20,59	MAIN	
FIL	2200 PFD FILM	1-20-0222	8	C30,31,34,41,42,44-46	MAIN	
FIL	0.022 MFD FILM	1-20-0223	4	C26-29	MAIN	
FIL	0.047 MFD FILM	1-20-0473	1	C15	MAIN	
HDW	6-32x1/4 PP BLK	5-00-0003	1	TO220 REG	MAIN	
HDW	4-24x1/4 PF ZNC	5-00-0009	4	SLIDE POT		
HDW	3-24x3/8 PP HILO	5-00-0013	4	LCD BEZEL		
HDW	4-24x5/16 PPB PLAST	5-00-1002	18	CASE/PCB		
HDW	1-72x3/16 SP	5-00-2001	4	SLIDE POT BRACKET		
HDW	#6 INT STAR WASHER	5-01-0002	1		MAIN	
HDW	1/2 STANDOFF 6-32	5-02-0003	1		MAIN	
HDW	SLIDE POT BRACKET	9-03-1016	2		· · · · ·	
HDW	WHITE VINYL STRIP	9-13-1007	2			
IC	7805 +5 V T0220	2-11-7805	1	U10	MAIN	NATIONAL ONLY
IC	78L12 +12 V T092	2-11-7803	1	U8	MAIN	NATIONAL ONLY
IC	79L12 -12 V T092	2-13-7912	1	U9	MAIN	NATIONAL ONLY
IC	74HC138	2-14-0138	1	U13	MAIN	NATIONAL ONE!
IC	74HC540	2-14-0540	1	U2	MAIN	
IC	74HC541	2-14-0540	1	U22	MAIN	
IC	74HC573	2-14-0541	1	U7	MAIN	
IC	74HC574	2-14-0573	2	U14,23	MAIN	
	74HC04	2-14-0374		,	MAIN	
IC IC			1	U6		
	TL084 (LF347)	2-21-0084	2	U20,21	MAIN	
IC IC	LM339	2-22-0339	1	U1	MAIN	DOA ONLY
IC IC	CD4052	2-23-4052	1	U19	MAIN	RCA ONLY
IC	6N138	2-24-0138	1	U13	MAIN	
IC	32Kx8 SRAM	2-17-0257	1	U12	MAIN	
IC	27C256 V1.09	2-19-0256	1	U11	MAIN	HR-16 ONLY
IC	27C256 V2.02	2-19-0256	1	U11	MAIN	HR-16B ONLY
IC	80C31	2-20-8031	1	U5	MAIN	
IC	PCM54HP DAC	2-25-0054	1	U18	MAIN	
IC	DM3 ASIC	2-27-0002	1	U17	MAIN	
IC	622 MASK ROM	2-27-0003	1	U15	MAIN	HR-16 ONLY
IC	623 MASK ROM	2-27-0004	1	U16	MAIN	HR-16 ONLY
IC	3B5 MASK ROM	2-27-0007	1	U15	MAIN	HR-16B ONLY
IC	3B6 MASK ROM	2-27-0008	1	U16	MAIN	HR-16B ONLY
JAC	5 PIN DIN JACK	4-00-0001	2	J2,3	MAIN	
JAC	1/4 CLIFF (MONO)	4-02-0001	5	J4,7-10	MAIN	
JAC	3.5mm JACK (P2)	4-16-0001	2	J5,6	MAIN	
JAC	3.5mm BAR JACK (P3)	4-16-0002	1	J1	MAIN	
LCD	LCD MODULE	9-44-1000	1			
LIT	USER'S MANUAL	7-51-1003	1		KYPD	
ME	1N4148 SIGNAL DIODE	2-00-4148	12	D6-14,17,20,21	MAIN	
ME	1N4001 POWER DIODE	2-01-4001	5	D1-5	MAIN	
ME	1N5231B ZENER	2-02-5231	1	D15	MAIN	METAL PACKAGE ONLY
ME	MPS 2369 TRANS.	2-03-2369	3	Q6,14,15	MAIN	
ME	2N4401 NPN TRANS.	2-03-4401	12	Q1-5,7-9,11,12,16,17	MAIN	
ME	2N4403 PNP TRANS.	2-04-4403	2	Q10,13	MAIN	
ME	LED (RED) RL55	3-02-0002	9		KYPD	
ME	PIEZO	7-00-0001	4		KYPD	
ME	12 MHz CER RES	7-01-0003	1	Z1	MAIN	
ME	LRG TORROID	7-30-0002	1	L1	MAIN	
ME	SM TORROID (1 WIRE)	7-30-0003	1	L2	MAIN	
ME	LITHIUM BATTERY	7-05-0001	1	B1	MAIN	
ME	DPDT SWITCH (ALPHA)	6-02-0001	1	SW1	MAIN	
MIS	REAR PANEL OVERLAY	9-13-1003	1			
MIS	RUBBER STRIP 8-3/4	9-23-1007	1			
PLS	CASE BOTTOM	9-11-1006	1			
PLS	KEY CAPS (WHT)	9-11-1007	16			HR-16 ONLY
PLS	KEY CAP (BLK)	9-11-1025	16			HR-16B ONLY
PLS	LCD BEZEL	9-11-1029	1			
PLS	SLIDE POT KNOB	9-11-1010	2			
PLS	ALPHA SWITCH CAP	9-11-1010	1			
POT	10K TRIMPOT	0-08-0103	1	R90	MAIN	
POT	10KB SLIDE POT MONO	0-09-1009	1	1100	IVICALIN	
POT	10KB SLIDE POT MONO	0-09-1009	1			
RES	100 1/8W 5%	0-09-1010	3	R75,120,133	MAIN	
						NOTES
GROUP	DESCRIPTION	PART#	QTY	POSITION	PCB	NOTES
RES	1K 1/8W 5%	0-00-0102	17	R23,29,35,36,48,49,50,51,64,67,69,72,91,92,112,114,115	MAIN	

RES	10K 1/8W 5%	0-00-0103	15	R5,30,32,39,52,53,82,86,97,99,103,104,106,113,121	MAIN
RES	100K 1/8W 5%	0-00-0104	5	R19,25,27,73,96	MAIN
RES	1M 1/8W 5%	0-00-0105	1	R31	MAIN
RES	10M 1/8W 5%	0-00-0106	1	R54	MAIN
RES	1.2K 1/8W 5%	0-00-0122	1	R38	MAIN
RES	15 1/8W 5%	0-00-0150	1	R116	MAIN
RES	1.5M 1/8W 5%	0-00-0155	1	R21	MAIN
RES	2K 1/8W 5%	0-00-0202	4	R65,66,70,71	MAIN
RES	200K 1/8W 5%	0-00-0204	3	R18,26,74	MAIN
RES	220 1/8W 5%	0-00-0221	19	R1-4,42-44,42-44,76-81,83-85	MAIN
RES	2.2K 1/8W 5%	0-00-0222	3	R41,123,124	MAIN
RES	3K 1/8W 5%	0-00-0302	2	R28,37	MAIN
RES	300K 1/8W 5%	0-00-0304	1	R63	MAIN
RES	3.3M 1/8W 5%	0-00-0335	1	R24	MAIN
RES	390K 1/8W 5%	0-00-0394	1	R17	MAIN
RES	470 1/8W 5%	0-00-0471	13	R7,68,117-119,125-132	MAIN
RES	4.7K 1/8W 5%	0-00-0472	16	R6,8,10,13-15,33,34,40,88,89,94,95,107,122,135	MAIN
RES	47K 1/8W 5%	0-00-0473	1	R11	MAIN
RES	470K 1/8W 5%	0-00-0474	1	R12	MAIN
RES	5.1K 1/8W 5%	0-00-0512	4	R100-102,105	MAIN
RES	51K 1/8W 5%	0-00-0513	1	R20	MAIN
RES	560 1/8W 5%	0-00-0561	4	R108-111	MAIN
RES	5.6K 1/8W 5%	0-00-0562	8	R55-62	MAIN
RES	820K 1/8W 5%	0-00-0824	1	R16	MAIN
RES	24K 8 PIN SIP	0-06-2438	1	R22	MAIN
RES	24K 9 PIN SIP	0-06-2439	1	R93	MAIN
RUB	TOP KEYPAD	9-21-1002	1		
RUB	BOT KEYPAD	9-21-1004	1		
RUB	ROUND RUBBER FEET	9-23-1004	4		
SOC	68 PIN ASIC SOCKET	4-12-0068	1	U17	MAIN

10.0 Software History

DATE VERSION	COMMENTS
11/1/87 1.01	First production release
12/1/87 1.02	 Fixes tape sync output so that when more than four drums are played on the same beat, the sync output pulse width does not change. Changed MIDI test routine so that an extra byte is sent out before testing MIDI to accommodate 8051s that have indeterminate data in the UART on power up.
12/14/87 1.03	 Fixes MIDI Song Pointer input bug that caused the HR-16 to continue from the wrong location if in song mode and a tempo was stored in the first step of the song. Fixes test routine display to read HR-16 instead of MMT-8.
12/16/87 1.04	1) Fixes cassette output bug that would occasionally cause a pattern to output data much longer than it should, which would make the cassette interface unusable.
12/30/87 1.05	 Fixes cassette input bug that would cause data to be corrupted if only pattern 99 is loaded in from tape. Fixes bug that would not recall the voice settings of a pattern after it had been loaded from tape (loading one pattern only). Previously, the pattern would have to be reselected after loading it from tape before the voices would recall their proper settings.
1/4/88 1.06	1) Fixes cassette input bug that would cause pattern 99 to be erased if a single pattern or song was loaded in, or a cassette was verified.
6/15/88 1.07	 Fixes bug that when adding beats to the beginning of a pattern, any drums more than one that occurred on beat 1 would remain on beat 1 instead of moving past the inserted beats. Fixes bug that would cause an incorrect display if aborting "LOAD ONE PART" before tape data has begun when previously in song mode, and aborting "LOAD ONE SONG" before tape data has begun when previously in part mode. Increased delay loops in display routines so that fewer LCD displays would be rejected in production. Added feature that allows MIDI program selection of patterns to work while a part is playing. If a new program number is received over MIDI, this program number will be selected to be the NEXT pattern number to play when the current pattern is finished. This functions exactly as if the new pattern number had been selected from the keypad. If a song is playing, MIDI program commands will still be ignored. Added feature that allows MIDI program change commands to select songs if the HR-16 is in song mode, and not playing. Previously, MIDI program change commands were ignored while in song mode. Revised service routines so that the DAC test can be entered directly by holding PATT and pressing VOICE while not in PLAY mode. The DAC test now plays a tom at low level once per second for easier calibration.
1.08	Not released.

- 8/25/88 1.09 1) Fixes bug that caused the HR-16 to send out an incorrect MIDI song position pointer if any tempo change steps occurred in the song previous to the current song position.
 - 2) Fixes bug that caused the HR-16 to send out an incorrect MIDI song position pointer if an empty pattern (8 beats, no drum events) was used in a step of a song previous to the current song position.
 - 3) Added feature that allows "spot erasing" while in record mode when quantize is off. This means that the erase button and a drum button can be held down while recording with quantize off in order to erase all drum events (quantized or not) that occur during the time that the buttons are held down.
 - 4) Added more steps of shuffle resolution, and changed the percentage display relationship to the clock. The original shuffle values and new values are shown below:

QUANT	OLD SHUFFLE	NEW SHUFFLE
1/4	0, 50%	0, 50%
1/6	0-16, 50%-75%	0-24, 50%-68.8%
1/8	0-12, 50%-75%	0-16, 50%-66.7%
1/12	0-8, 50%-75%	0-12, 50%-68.8%
1/16	0-6, 50%-75%	0-8, 50%-66.7%
1/24	0-4, 50%-75%	0-6, 50%-68.8%
1/32	0-3, 50%-75%	0-4, 50%-66.7%
1/48	0-1, 50%-62.5%	0-2, 50%-62.5%
1/64	0, 50%	0-1, 50%-58.3%
OFF	0, 50%	0,50%

Despite the displayed percentage being smaller in the new values, there are actually more shuffle steps than before. The old displayed percentages represented the ratio between the clock location of the shuffled beat, and the clock location half way between two un-shuffled beats. The new percentage represents the percentage of the total time of two occurring beats that the first of a shuffled pair will take. For example, 1/16 notes set to shuffle 8 (shifting every other 16th note 8 clocks late), will result in the first 16th note getting 32 clocks, and the second 16th note getting 16 clocks (instead of 24 each when shuffle=0). This results in the first 16th note getting 66.7% of the total time of both 16th notes (32/48=66.7%), which is equivalent to 16th note triplets. This percentage representation is more useful than the old percentage.

:/:/09	2.00	 Fixes lots o' bugs. Add lots o' features.
?/?/90	2.01	HR-16/B only: 1) Changed JAM BLOCK name to BLOCK.

HR-16 and HR-16/B:

HR-16 and HR-16/R.

- 1) Fixed bug which caused single step with swing on to advance in incorrect amounts. If swing was advanced by 1 while in 16th not quantize, the steps would be 23/96, 48/96, 71/96 instead of 25/96, 48/96. 73/96. This is now fixed.
- 2) Added copyright notice on power on.

3/10/92 2.03 HR-16 and HR-16/B:

2/2/20

7/3/90

2.00

2.02

- 1) Fixed bug which caused a wrong amount of silence at the beginning of a pattern if its length was changed to a shorter value from the top and there was no drum event on the old or new downbeat. For example, if no events existed on beats 1 and 2, and the length from top was changed to be shorter by one beat, the amount of silence before the first event would be wrong.
- 2) Fixed bug which caused sysex loading to be garbled if any real-time MIDI information was received during the sysex dump. This seemed to only be a problem with IBM MPU-401 interfaces.
- 3) All individual's names have been removed from the software.

11.0 MIDI Implementation

ALESIS HR-16/HR-16B MIDI SYSTEM EXCLUSIVE FORMAT

The following information is provided as a guide for programmers wishing to modify the data received via MIDI from the HR-16 for the purpose of interchanging patterns from separate block dumps, modification of drum setups, MIDI channel assignments, etc. Great care must be taken to insure that all modified addresses are valid, since one incorrect value (the length of a pattern, for example) could result in all data being lost in the HR-16. These errors may not show up immediately, since the incorrect values may not be accessed by the HR-16 until a particular pattern or song is selected. Therefore, it is recommended that any data manipulation programs be thoroughly tested after loading into the HR-16 by selecting and recording on many patterns and songs before assuming that the data is valid.

For any of the sysex commands to be transmitted or received, the SYSEX ENABLE function (MIDI/UTIL page 15) must be turned on. All 11 possible commands will be transmitted in the following format:

HEX	COMMENTS
F0H	SYSTEM EXCLUSIVE STATUS BYTE
00H	
00H	
0EH	ALESIS I.D. NUMBER
01H	HR-16 I.D. NUMBER
00H-0AH	SYSEX COMMAND
•••	DATA
F7H	EOX

The following sysex commands are transmitted and received by the HR-16:

00H COMPLETE MEMORY DUMP

A system exclusive MIDI data dump from the HR-16 is initiated by holding the TAPE button down, pressing (and releasing) the left arrow button once, and then pressing the RECORD button. This command is followed by a block of data representing the contents of the HR-16's memory. In order to optimize the data transfer, 8 MIDI bytes are used to transmit each block of 7 HR-16 data bytes. If the 7 data bytes are looked at as one 56-bit word, the format for transmission is eight 7-bit words beginning with the most significant bit of the first byte, as follows:

SEVEN HR-16 BYTES:								
0:	A7	A 6	A5	A4	А3	A2	A1	A0
1:	В7	В6	В5	B4	В3	B2	В1	B0
2:	C7	C6	C5	C4	C3	C2	C1	C0
3:	D7	D6	D5	D4	D3	D2	D1	D0
4:	E7	E6	E5	E4	E3	E2	E1	ΕO
5 :	F7	F6	F5	F4	F3	F2	F1	F0
6:	G7	G6	G5	G4	G3	G2	G1	G0

	TRANSMITTED AS:								
0:	0	Α7	A 6	A5	A4	А3	A2	A1	
1:	0	ΑO	В7	В6	В5	B4	В3	В2	
2:	0	В1	ВO	C7	C6	C5	C4	C3	
3:	0	C2	C1	C0	D7	D6	D5	D4	
4:	0	D3	D2	D1	D0	E7	E6	E5	
5 :	0	E4	E3	E2	E1	E0	F7	F6	
6:	0	F5	F4	F3	F2	F1	FΟ	G7	
7:	0	G6	G5	G4	G3	G2	G1	G0	

In order to use the data properly, it must be decoded properly into HR-16 byte format. The following list gives the data locations within the "unpacked" (decoded) block of data, starting with the first byte of the block being 000. NOTE: All absolute addresses must have an offset of 8200H added to them (e.g., an absolute pointer to a pattern that starts at 35AH should have the pointer value 855AH).

000H-0C7H	DON'T CARE
0C8H	MIDI channel
0C9H	Receive MIDI drum triggers (0=off, 1=on)
0CAH	Transmit MIDI drum triggers (0=off, 1=on)
0CBH	MIDI note assignment of CLICK (0-127)
0CCH	MIDI note assignment of KICK (0-127)
0CDH	MIDI note assignment of SNARE (0-127)
0CEH	MIDI note assignment of CLS HAT (0-127)
0CFH	MIDI note assignment of MID HAT (0-127)
0D0H	MIDI note assignment of OPEN HAT (0-127)
0D1H	MIDI note assignment of CLAPS (0-127)
0D2H	MIDI note assignment of PERC 3 (0-127)
0D3H	MIDI note assignment of PERC 4 (0-127)
0D4H	MIDI note assignment of TOM 1 (0-127)
0D5H	MIDI note assignment of TOM 2 (0-127)
0D6H	MIDI note assignment of TOM 3 (0-127)
0D7H	MIDI note assignment of TOM 4 (0-127)
0D8H	MIDI note assignment of RIDE (0-127)
0D9H	MIDI note assignment of CRASH (0-127)
0DAH	MIDI note assignment of PERC 1 (0-127)
0DBH	MIDI note assignment of PERC 2 (0-127)
0DCH	MIDI echo (0=off, 1=on)
0DDH	MIDI program select (0=off, 1=on)
0DEH	Clock mode (0=MIDI & internal, 1=internal only, 2=tape)
0DFH	MIDI clock out (0=off, 1=on)
0E0H	Auto start (0=off, 1=on)
0E1H	Click value
0E2H	Click in play (0=off, 1=on)
0E3H	Manual voice/tune/mix (0=off, 1=on)
0E4H	Pad dynamics (0-0AH)
0E5H	Song loop (0=off, 1=on)
0E6H	Sysex enable (0=off, 1=on)
0E7H-0EBH	Software version: 5 ascii bytes, starting with a space (20H) if an HR-16, or a "B" (42H) if an
	HR-16B, followed by a 4 digit version number (e.g., "2.00", or 32H, 2EH, 30H, 30H)
0ECH-F3H	DON'T CARE
0F4H	0

DON'T CARE

0F5H-FDH

```
0FEH
             27H
0FFH
             0B5H
100H-187H
             DON'T ALTER(this can be DON'T CARE if manual voice/tune/mix is off)
188H-191H
             DON'T CARE
192H-1A1H
             0
1A2H-1FFH DON'T CARE
200H
             MSB of absolute pointer to pattern 00
             LSB of absolute pointer to pattern 00
201H
             MSB of absolute pointer to pattern 01
202H
             LSB of absolute pointer to pattern 01
203H
             MSB of absolute pointer to pattern 02
204H
             LSB of absolute pointer to pattern 02
205H
             MSB of absolute pointer to pattern 99
2C6H
             LSB of absolute pointer to pattern 99
2C7H
2C8H-2CCH DON'T ALTER
2CDH
             LSB of absolute pointer to first byte past SONG 99 data
2CEH
             MSB of absolute pointer to first byte past SONG 99 data
2CFH-2D0H DON'T ALTER
             LSB of FF00H minus data in 0CDH & 0CEH
2D1H
             MSB of FF00H minus data in 0CDH & 0CEH
2D2H
2D3H-2D4H DON'T ALTER
             Shuffle amount (0-24, 0=50%)
2D5H
2D6H-2D7H DON'T ALTER
2D8H
             Tempo (20-255)
2D9H
             Quant clock count (must correspond to Quant value 0-9: 96, 64, 48, 32, 24, 16, 12, 8, 6, 1)
2DAH
             Quant value (0-9)
2DBH-2FFH DON'T CARE
300H-301H
             DON'T ALTER
             MSB of absolute pointer to song 00
302H
             LSB of absolute pointer to song 00
303H
304H
             MSB of absolute pointer to song 01
305H
             LSB of absolute pointer to song 01
306H
             MSB of absolute pointer to song 02
             LSB of absolute pointer to song 02
307H
3C8H
             MSB of absolute pointer to song 99
3C9H
             LSB of absolute pointer to song 99
3CAH-3CCH DON'T ALTER
3CDH-3D2H DON'T CARE
3D3H-3D6H DON'T ALTER
```

The pattern and song data must be dealt with in a specific manner:

1) All pattern and song data must be in consecutive order, i.e., pattern 05 data cannot be before pattern 02's data. The order for the data should be pattern 00 through 99, followed by song 00 through 99.

DON'T CARE

PATTERN 00 DATA

3D7H-3FFH

400H-?

- 2) If a pattern or song does not exist, its MSB pointer will = 0, which is an illegal pointer address. Since there will be no data for this pattern, it is skipped, i.e., if pattern 04 is empty, pattern 05's data follows after pattern 03's data.
- 3) There can be no gaps in the data. Pattern 01's data must follow directly after pattern 00's data, etc.
- 4) Locations 2CDH-2CEH (start of free memory) and 2D1H-2D2H (length of free memory) must be kept valid.
- 5) Song 99 MUST exist. This means that at least an empty song (03H 00H FFH) must be at the end of memory, and song 99 must point to it.
- 6) It is suggested that all DON'T CARE data be left in the state that it is received in, although these locations can be replaced with zeroes.

PATTERN DATA FORMAT

The following is the format of each pattern, starting with the address pointed to byte the absolute pointer to the pattern (offset by 8200H):

00H	LSB of number of bytes in pattern, including header.
01H	MSB of number of bytes in pattern, including header.
02H	LSB of number of beats in pattern in BCD format (0 beats =
03H	MSB of number of beats in pattern in BCD format empty pattern)
04H	KICK sound number (0-30H)
05H	KICK output assign (bit 7) and volume (bits 0-6: 0-63H)
06H	KICK panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
07H	SNARE sound number (0-30H)
08H	SNARE output assign (bit 7) and volume (bits 0-6: 0-63H)
09H	SNARE panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
0AH	CLS HAT sound number (0-30H)
0BH	CLS HAT output assign (bit 7) and volume (bits 0-6: 0-63H)
0CH	CLS HAT panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=15)
0DH	MID HAT sound number (0-30H)
0EH	MID HAT output assign (bit 7) and volume (bits 0-6: 0-63H)
0FH	MID HAT panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=15)
10H	OPN HAT sound number (0-30H)
11H	OPN HAT output assign (bit 7) and volume (bits 0-6: 0-63H)
12H	OPN HAT panning (bits 5-7: 0=L,6=R) & pitch (bits 0-4:0=-16, 1FH=15)
13H	CLAPS sound number (0-30H)
14H	CLAPS output assign (bit 7) and volume (bits 0-6: 0-63H)
15H	CLAPS panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
16H	PERC 3 sound number (0-30H)
17H	PERC 3 output assign (bit 7) and volume (bits 0-6: 0-63H)
18H	PERC 3 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
1077	
19H	PERC 4 sound number (0-30H)
19H 1AH	PERC 4 sound number (0-30H) PERC 4 output assign (bit 7) and volume (bits 0-6: 0-63H)
1AH	PERC 4 output assign (bit 7) and volume (bits 0-6: 0-63H)
1AH 1BH	PERC 4 output assign (bit 7) and volume (bits 0-6: 0-63H) PERC 4 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
1AH 1BH 1CH	PERC 4 output assign (bit 7) and volume (bits 0-6: 0-63H) PERC 4 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15) TOM 1 sound number (0-30H) TOM 1 output assign (bit 7) and volume (bits 0-6: 0-63H) TOM 1 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
1AH 1BH 1CH 1DH 1EH 1FH	PERC 4 output assign (bit 7) and volume (bits 0-6: 0-63H) PERC 4 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15) TOM 1 sound number (0-30H) TOM 1 output assign (bit 7) and volume (bits 0-6: 0-63H) TOM 1 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15) TOM 2 sound number (0-30H)
1AH 1BH 1CH 1DH 1EH	PERC 4 output assign (bit 7) and volume (bits 0-6: 0-63H) PERC 4 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15) TOM 1 sound number (0-30H) TOM 1 output assign (bit 7) and volume (bits 0-6: 0-63H) TOM 1 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)

```
22H
             TOM 3 sound number (0-30H)
23H
             TOM 3 output assign (bit 7) and volume (bits 0-6: 0-63H)
             TOM 3 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
24H
25H
             TOM 4 sound number (0-30H)
             TOM 4 output assign (bit 7) and volume (bits 0-6: 0-63H)
26H
27H
             TOM 4 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
             RIDE sound number (0-30H)
28H
29H
             RIDE output assign (bit 7) and volume (bits 0-6: 0-63H)
2AH
             RIDE panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
             CRASH sound number (0-30H)
2BH
             CRASH output assign (bit 7) and volume (bits 0-6: 0-63H)
2CH
             CRASH panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
2DH
2EH
             PERC 1 sound number (0-30H)
             PERC 1 output assign (bit 7) and volume (bits 0-6: 0-63H)
2FH
30H
             PERC 1 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
             PERC 2 sound number (0-30H)
31H
             PERC 2 output assign (bit 7) and volume (bits 0-6: 0-63H)
32H
             PERC 2 panning (bits 5-7: 0=L, 6=R) & pitch (bits 0-4:0=-16, 1FH=+15)
33H
34H-??
             PATTERN DATA
             OFFH (End of pattern)
??
```

Pattern data must follow these rules:

- 1) Each byte of the pattern data (from 34H on) is either a drum event, or a count of clocks to wait, or 0FFH, which indicates the end of the pattern. If the event is a drum event, bit 7 will be 0, bits 4-6 will contain the dynamics of the note (0-7), and bits 0-3 will contain the drum to be played (0-15, in the same order as above). If the event is a count of clocks, bit 7 will be high, and bits 0-6 will indicate the number of clocks to wait (0-126). A wait of 0 clocks is legal, and will cause the pointer to immediately advance to the next event. An empty 8 beat pattern would consist of the following pattern data: 0FEH, 0FEH, 0FEH, 0FEH, 0FEH, 0FEH, 0FEH, 0FFH. This data will count clocks for 126*6+12 clocks (768 clocks, divided by 96 clocks per beat = 8 beats), after which it will loop around since it has reached the end of the pattern.
- 2) Adding the number of bytes in a pattern to the absolute pointer of a pattern should point to 1 byte past the last byte of the pattern.

SONG DATA FORMAT

The following is the format of each song, starting with the address pointed to by the absolute pointer to the pattern (offset by 8200H):

00H	LSB of number of bytes in song, including header.
01H	MSB of number of bytes in song, including header.
02H	Step 1
03H	Step 2
04H	Step 3
05H	Step 4
06H	etc
xxH	Pattern number 0FFH (end of song)

Song data must follow these rules:

- 1) Step data 0-99 indicate pattern steps. Step data 100-250 indicate tempo change of 50% to 200%, respectively. Step data of 251-254 are not accessible from the front panel, but would correspond to tempos of 201% through 204%.
- 2) There cannot be more than 255 steps in a song.
- 3) Adding the number of bytes in a song to the absolute pointer of a song should point to 1 byte past the last byte of the song.

01H SELECT PATTERN OR SONG

This command is used to select a pattern or song.

0000000xB x: 0=pattern, 1=song

0nnnnnnB n: 0-99 = pattern or song number

7FH EOX

02H RECORD BUTTON

This command is used to "press" or "release" the RECORD button. It will affect whether the HR-16 will go into play or record when it receives a MIDI START command. It does not affect what will happen when pressing play from the front panel.

0000000xB x: 0=Record released, 1=Record pressed

F7H EOX

03H QUANTIZE AND SWING MODES

This command is used to set the quantize and swing modes.

quantize mode 0=1/4, 1=1/6, 2=1/8, 3=1/12, 4=1/16, 5=1/24, 6=1/32,

......7=1/48, 7=1/64, 9=1/384

000nnnnnB nnnnn: 0-24 =swing amount, 0=50%

F7H EOX

04H SET PATTERN LENGTH

This command is used to change the length of the current pattern.

0t0ccccbB t: 0=change end, 1=change top

ObbbaaaaB ccccbbbbaaaa: 3 digit BCD length in beats (c=msb, a=lsb)

F7H EOX

05H COPY PATTERN, DRUM, OR SONG

This command is used to copy a pattern to another pattern, a drum to a pattern, or a song to a song. If the command is to copy a pattern, the data received will be appended to the end of the currently selected pattern. If the command is to copy a song, the data received will be appended to the end of the currently selected song. If the command is to copy a drum, the drum number sent in the mode byte (-1) will be copied to the drum button hit within 3 seconds of receiving this command, otherwise it will be ignored.

000000xxB x: MSB of number of unpacked bytes of data after header 0xxxxxxyB y: LSB of number of unpacked bytes of data after header

0yyyyyyB if y_0 , then x=x+1

000nnnnnB n: copy mode: 0=copy patt, 1-16=copy drum, 17=copy song
The data is packed as 8 MIDI bytes per 7 data bytes as described above in the MIDI bulk dump explanation. It contains a complete

pattern or song.

00000000B This extra byte is required for proper operation

F7H EOX

When transmitting any copy function, it is recommended that a pause of one second be inserted between the copy mode byte and the data that follows it to insure that the receiving HR-16 has enough time to move memory around to make room for the new pattern or song. In addition, it is recommended that a delay be added before sending additional MIDI commands, since it may take a few seconds for the copy operation to be complete, during which time MIDI data will be ignored. The amount of time required will be dependent on the length of the patterns or songs being copied, and the amount of free memory available.

06H STEP EDIT MODE

This command is used to enter or exit step edit mode, as well as for stepping through the edited pattern. If it is received while in song mode, it will be ignored. If a step command is given while not in step mode, it will also be ignored. The HR-16 will always transmit the current quantize and swing settings before sending an enter step command. When receiving a step to next beat, any additional drums on the existing beat will be skipped. When receiving a step to next drum command when currently on the last drum of a beat, the command will be ignored.

000000xxB x: 0=enter step mode, 1=exit step mode, 2=step to next beat, 3=step to next drum

F7H EOX

07H REQUEST SYSEX DUMP

This command is used to request a complete sysex memory dump from the HR-16. After receiving this command (if not in PLAY mode), the HR-16 will send out its complete memory via MIDI.

F7H EOX

08H CHANGE VOICE, TUNE, MIX SETTINGS

This command is receive only, and is used to change the voice settings of the current pattern. It can function while the pattern is playing, and will update the display if the settings being displayed are

changed. It will be ignored if in song mode. The format is packed as 8 MIDI bytes per 7 data bytes as described in the MIDI bulk dump explanation. The data is identical to bytes 4 through 33H in the pattern data format.

data 48 data bytes, transmitted as 55 MIDI bytes

F7H EOX

09H MIDI COMMUNICATIONS TEST

This command is used to insure that bi-directional MIDI communication is functioning. If an HR-16 receives the inquiry command (F0H, 00H, 00H, 00H, 01H, 09H, 00H, F7H), it will respond with the response command (F0H, 00H, 00H, 01H, 01H, 09H, 01H, F7H) only if MIDI ECHO is turned off. If MIDI ECHO is on, the transmitting device will see the inquiry message returned to it if bi-directional communication is functioning. This function is useful in determining that the HR-16 is ready to receive additional MIDI information. For example, selecting a pattern, or copying a pattern can cause a delay in which the HR-16 will ignore incoming MIDI information if its input buffer overflows. By sending this command after a copy pattern command (command 5), and then waiting for the response before sending any additional commands, it can be insured that the HR-16 will not miss any information.

0000000xB x=0=MIDI inquiry, x=1=MIDI response

F7H EOX

0AH ERASE PATTERN OR SONG

This command is used to erase the currently selected pattern or song. It will be ignored if in play mode.

F7H EOX

12.0 Service Manual History

7/27/95

V1.00

1st release.

<u>INDEX</u>

+	C3, 1	Instruction latch strobe, 5
+12V, 1, 2	C34, 6, 18	Instruction reset strobe, 5
+5V, 1, 3, 15		internal diagnostics, 8
-	C4, 1, 18	
-12V, 1	C47, 12	J J1, 1, 18
1	C5, 1, 15, 18	J11, 6, 18
1/4 inch jacks, 6	C50, 6	
1/8 inch cable, 8	C59, 2	J12, 11, 18
12MHz, 3	C6, 1, 18	J5, 16, 18
1N5231B, 9, 18	C62, 3, 14	J6, 16
4	C64, 3	jitter, 6
4052, 6, 16, 18	C65, 3	jumper, 10, 11, 13, 15
5	C7, 1	K
5.1V zener, 3	CA, 1, 9, 10, 11, 12, 13, 14, 15	keypad, 3, 4, 6, 12, 16, 18, 19, 20
6 6MHz, 5	cassette, 6, 20	L LCD, 3, 4, 11, 15, 18, 20
	CE, 5, 10, 16	LED Test, 8
7 74HC04, 10, 18	ceramic disk, 12, 13, 15	Lithium, 2, 18
74HC04s, 6	chokes, 13	lock-up, 3
74HC138, 4, 15, 18	Click value, 24	•
74HC540, 6, 18	cliff jack, 10	low order address, 3
7805, 1, 18	CLOCK, 3, 5, 10, 15, 21, 24, 25	low power, 2, 13
	comparators, 6	LSI, 5
7812, 1, 18		M Manual voice/tune/mix, 24, 25
7912, 1, 18	contacts, 10, 12, 16	Mask Rom, 5, 17, 18
8 8031, 3, 4, 5, 6, 7, 8, 10, 11, 13, 15, 16, 18	COPY, 29, 30	mask ROMs, 5
A	crashes, 10, 16, 17	
A, 1, 4, 6, 7, 9, 10, 11, 12, 13, 15, 23, 27	D D1, 1, 18	MD0-MD7, 5
A0-A19, 5	D15, 3, 4, 15, 18	MEM PWR, 2
A15, 4	D19, 6	MEMORY DUMP, 23, 29
A8-A10, 4	D2, 1, 18	memory mapped I/O, 3, 4
adapter, 1	D21, 11	microprocessor, 1
adapters, 7	D3, 1	MIDI, 3, 4, 8, 11, 15, 16, 20, 21, 22, 23, 24, 28, 29, 30
ADC, 16		mono, 10, 18
Address Buss, 5, 8, 15	D4, 1	monolithic block ram capacitors, 12, 13
adjustment, 6, 8, 9, 17	D5, 1, 15	Most Significant Bit, 6, 23
Analog switch, 6, 16	D6, 4, 18	N
analog to digital, 6	D7, 2, 5	noise, 2, 3, 7, 8, 11, 12, 13, 14
AQ, 1, 6, 9, 10, 11, 13, 15, 16, 18	D8, 9	normaling, 10
ASIC, 3, 4, 5, 6, 10, 15, 16, 17, 18, 19	DAC, 5, 6, 8, 11, 16, 17, 18, 21	0
audio test, 8	DAC0-DAC16, 5	OE, 10
Auto start, 24	data buss, 2, 3, 4, 5, 10, 15, 16, 17	op-amp, 3, 16, 17
B	data corruption, 2, 3, 9	opto isolator, 4, 11
Battery backup, 2, 3, 8, 12, 16	data slider, 6, 16, 17	oscillation, 3
battery drain, 2, 12	DataDisk, 7	Output Sample and Hold, 5
binary weighted resistor network, 6, 16	distortion, 13	output section, 6
button failures, 4	DM3AG, 3, 5, 6, 15, 16, 17	Oxidation, 7, 10
buzz, 8	drift, 12	oxidize, 12
bypass, 1, 14, 15, 16	dropouts, 7	Р
C	E	PATTERN DATA, 26, 27, 30
C1, 1, 18	EPROM, 3, 8, 10, 15, 16, 17	PCM-54, 6, 8, 12, 16, 17
C11, 13, 16, 18	H hot glue, 13	piezo, 3, 6, 16, 18
C16, 6, 18	HR-16, 3, 5, 6, 7, 8, 11, 12, 15, 17, 18, 20,	power supply, 1, 13, 14, 15, 17
C2, 1	21, 22, 23, 24, 28, 29, 30	program, 3, 20, 24
C20, 3, 12	HR-16B, 17, 18, 23, 24	program change, 21
C23, 13, 16	1	pullup resistor, 4, 7, 16
	I/O, 3, 4, 6, 8, 15, 17	
UD 16/UD16D Convice Manual 1	00 22	

DUD 2 44 47	D00 6 9 49	tone input 6 0 12
PUP, 2, 14, 17	R90, 6, 8, 18	tape input, 6, 8, 13
Q Q1/Q2, 4	R96, 3	Tape output, 6, 7
Q10, 2, 18	R97, 2	tape sync, 6, 20
Q11, 2	R99, 3	threshold, 3, 4, 11, 12, 13, 16
Q12-Q13, 3	RAM Test, 8	TOM 1, 16, 24, 26
Q3, 6	raw +10V, 1, 3	TOM 3, 16, 24, 27
Q4, 3	read, 3, 6, 10, 20	trimpot, 6, 8, 11, 18
Q5, 3	reinitializing, 8	troubleshooting, 3, 15
·	reset, 1, 2, 3, 12, 13, 15, 16	TXD, 3, 4, 11
QUANTIZE, 21, 22, 28, 29	ribbon cable, 16	U
R R.F., 1, 10, 11, 13	ROM Test, 8	U1, 3, 6, 16, 18
R.F. suppression, 1	RXD, 3	U10, 1, 18
R10, 3	S	U11, 3, 18
R100, 3, 19	\$1,1	U13, 4, 15, 18
R105, 3	samples, 5	U14, 4, 18
R110, 10	self test, 8	U19, 6, 18
R133, 13	shield, 11	U2, 6, 18
R16-R20, 6	shorts, 1, 11	U20, 2, 6, 14, 16, 18
	SHUFFLE, 21, 25	U21, 6, 16
R22, 6, 19	SIP, 6, 19	U22, 4, 18
R23, 6, 19	SNH0, 5	U3, 6
R24, 3, 12, 19	SNH1, 5	U4, 4, 16
R25, 3	SNHIN, 5	U6, 10, 13, 18
R27, 3	software history, 15	U8, 1, 18
R28, 3, 13, 16, 19	solder mask, 10, 11	U9, 1, 18
R29, 3	SONG DATA, 25, 26, 27, 28	update, 10, 30
R30, 3	Song Pointer, 20	user error, 6, 15, 16
R41, 12, 19	SRAM, 1, 2, 3, 8, 9, 15, 16, 18	V
R5, 4, 11, 16, 19	SRAMs, 2, 9	Vcc, 15
R52, 6	standby current, 2	velocity, 6, 16
R53, 6	STB, 5	voltage doubler, 1
R54, 6, 19	steering diode, 2	volume slider, 6, 13, 16, 17
R6, 4, 11, 19	STEP EDIT, 29	W
R60, 12	stereo panning, 6	wave shaping, 6, 7
R63, 6, 19	STRES, 5	write, 3, 4
R68, 6	SYSEX, 22, 23, 24, 29	Z Z1, 3, 18
R7, 4, 11, 19	Т	, -,

tape backup, 6

R73-R75, 6

NOTES