## Service Manual

B PARTS LIST
(without price)


## JUNE 1985



## CAUTION:

When the connector (from the batteries) is disconnected, all the sound data in the Memory Bank are cleared. When this happens, initialize the unit by the following procedures.

1. Turn the power switch off and press INITIALIZE button.
2. Turn the power switch on, then the display indicates;

3. While pushing INITIALIZE button, press YES button on the data entry section of the panel. All the Memory Bank data are initialized, then the display shows:


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## 1. SCHEMATIC DIAGRAM

1-1. Main PCB (A) M5153-MA1M









1-9. Modulation Switch PCB M5153-CN3





2. WIRING DIAGRAM


NOTE: 1. Wire Color Codes

| R : Red | W: White | BL: Blue |
| :--- | :--- | :--- |
| Y: Yellow | GR: Green | PP: Purple |
| BK: Black | BR: Brown | $\mathrm{O}:$ Orange |
| GY: Gray | PK: Pink | $E:$ Shielded wire |

2. Terminal Readings


Connected to PCB MA-3M through a brown wire


Connected to Connector D pin 2 on PCB AS-1M
3. Voltage Levels


## 3. PCB VIEW \& MAJOR CHECKPOINT

## 3-1. PCB M5153-MA1M




## 4. MAJOR WAVEFORMS

Notes: Photographs marked (M) show stored waveforms in a memory scope.
The analog waveforms were observed via a 28 Kohm resistor.


(1)
$\mu$ PD7811 clock pulse PCB M5153-MA1M 74HCU04-1 pin 6 $0.1 \mu \mathrm{~s} / \mathrm{div} ., 2 \mathrm{~V} / \mathrm{div}$.

DOE
PCB M5153-MA1M $\mu$ PD933 pin 22
$10 \mu \mathrm{~s} / \mathrm{div}$., $5 \mathrm{~V} / \mathrm{div}$
Tone: Flute, Key: C4
(4) DAC output PCB M5153-MA1M TL082-こ pin 7 $10 \mu \mathrm{~s} / \mathrm{div} ., 5 \mathrm{~V} / \mathrm{div}$. Tone: Flute, Key: C4


(2) $\mu \mathrm{PD} 933$ clock pulse PCB M5153-MA1M $74 \mathrm{HCU} 04-2$ pin 2 $0.1 \mu \mathrm{~s} / \mathrm{div} ., 2 \mathrm{~V} / \mathrm{div}$.

(5) DOE and (6) DAC outputs

Same conditions as (3) and (4) except $2 \mathrm{~ms} / \mathrm{div}$. of sweep time and using a memory scope.

(7) DAC output

PCB M5153-MA1M
TL082-3 pin 7
$2 \mathrm{~ms} / \mathrm{div}$., $5 \mathrm{~V} / \mathrm{div}$.
Tone: Flute, Key: C4
(8) Expander Circuit output

PCB M5153-MA1M
TL082-3 pin 1
$2 \mathrm{~ms} / \mathrm{div}$., $0.5 \mathrm{~V} / \mathrm{div}$.
Tone: Flute, Key: C4

(11) Master LSI DOE signal PCB M5153-MA1M $\mu$ PD933-1 pin 22 $10 \mu \mathrm{~s} / \mathrm{div}$., $2 \mathrm{~V} / \mathrm{div}$.
(12) Master LSI SH signal PCB M5153-MA1M $\mu$ PD933-2 pin 23 $10 \mu \mathrm{~s} / \mathrm{div} ., 2 \mathrm{~V} / \mathrm{div}$.

(9) DAC output and (10) Expander Circuit output
Same conditions as (7) and (8) except using a memory scope.

(13) Master LSI SH signal

PCB M5153-MA1M
$\mu$ PD933-1 pin 23
$0.1 \mu \mathrm{~s} / \mathrm{div}$., $2 \mathrm{~V} / \mathrm{div}$.
(14) Sample \& Hold Circuit output

PCB M5153-MA1M
TL082-2 pin 7
$0.1 \mu \mathrm{~s} / \mathrm{div} ., 2 \mathrm{~V} / \mathrm{div}$.
Tone: Flute, Key: C7

(15) Master LSI SH signal

PCB M5153-MA1M
$\mu$ PD933-1 pin 23
$10 \mu \mathrm{~s} / \mathrm{div} ., 2 \mathrm{~V} / \mathrm{div}$.
(16)

Slave LSI SH signal PCB M5153-MA1M $\mu$ PD933-2 pin 23 $10 \mu \mathrm{~s} / \mathrm{div} ., 2 \mathrm{~V} / \mathrm{div}$.

(19)

Mixed 0.54 Hz and 6.1 Hz signals PCB M5153-MA2M

Anode of VCO input diode $1 \mathrm{~s} / \mathrm{div}$., $1 \mathrm{~V} / \mathrm{div}$.

(17) 0.54 Hz LFO output PCB M5153-MA2M
TC4069-1 pin 4
0.5s/div., 2V/div.
(18) 6.1 Hz LFO output

PCB M5153-MA2M
TC4069-1 pin 6
$0.5 \mathrm{~s} / \mathrm{div} ., 2 \mathrm{~V} / \mathrm{div}$.

(20) Filter A output

PCB M5153-MA2M
NJM4558-2 pin 7
$2 \mathrm{~ms} /$ div., $0.5 \mathrm{~V} / \mathrm{div}$.
(21) BBD output

PCB M5153-MA2M
MN3209-1 $\operatorname{pin} 7$
$2 \mathrm{~ms} / \mathrm{div}$., $0.5 \mathrm{~V} / \mathrm{div}$.

6. DIGITAL CIRCUIT BLOCK DIAGRAM


Function of each block:
MAIN CPU - Controls keys and switches scanning, sequencer, MIDI and cassette tape player.
SUB-CPU - Mainly controls Music LSIs.
CPU Interface - Interfaces between MAIN CPU and SUB-CPU.
Main RAM 1 - The first 2K bytes are for system execution and the rest of 6 K bytes store the sequencer data.
Main RAM 2 - Stores the sequencer data.
Sub-RAM 1 - Having 2K-byte capacity, stores tone data for Memory Banks $A$ and $B$.
Sub-RAM 2 - System execution area.
Sub-RAM 3 - Stores data fro Memory Banks C and D.
7. MAIN CPU ( $\mu$ PD7811-180)

| PIN NO. | TERMINAL NAME | IN/OUT | FUNCTION |
| :---: | :---: | :---: | :---: |
| $1 \sim 8$ | PAO (S) ~PA7 (S7) | IN/OUT | Data bus for LCD and RAM pack. PA0~PA3 also generate key common signals. |
| 9 | PBO (SYNC) | IN | Synchronous signal from CPU Interface (MB64H173) |
| 10 | PB1 (MT-0) | OUT | Serial data output for cassette tape |
| 11 | PB2 (INT) | OUT | SUB-CPU interrupt signal |
| 12 | PB3 (CONT) | IN/OUT | Control signal between MAIN and SUB-CPUs |
| 13 | PB4 (MT-I/O) | OUT | Remote control (start, stop) signal for cassette tape recorder |
| 14 | PB5 (B5) | OUT | LCD unit control signal |
| 15 | PB6 (B6) | OUT | LCD Driver LSI chip select signal |
| 16 | PB7 (B7) | OUT | LCD Driver LSI Read/ $\overline{\text { Write }}$ signal |
| 17 | PCO (M-OUT) | OUT | MIDI (Musical Instrument Digital Interface) data output |
| 18 | PC1 (M-IN) | IN | MIDI data input |
| 19 | PC2 (CE) | OUT | RAM Pack (option) chip select signal |
| 20 | PC3 (MT-1) | IN | Data input from cassette tape |
| $21 \sim 24$ | PC4 ~ PC7 | OUT | Metronome (timing signal for music recording) pitch signals |
| 26 | INT1 | IN | Interrupt from SUB-CPU |
| 28 | $\overline{\text { RESET }}$ | IN | Initializes the LSI's internal circuits at Power ON. |
| 31 | X1 | IN | 12 MHz clock pulse |
| 32 | VSS | IN | Logic ground ( OV ) source |
| 33 | AVSS | IN | Ground for the built-in ADC (Analog to Digital Converter) |
| 34 | ANO | IN | Bender wheel input. A voltage from the bender wheel is converted into digital data by a built-in ADC. |
| 35 | AN1 | IN | Modulator wheel input. A voltage from the modulator wheel is converted into digital data by a built-in ADC. |
| 42 | VREF | IN | Reference voltage ( +5 V ) for the built-in ADCs |


| 43 | AVCC | IN | +5 V power source for the built-in ADCs |
| :---: | :---: | :---: | :---: |
| 44 | $\overline{\mathrm{RD}}$ | OUT | Read signal. Drops to " $L$ " when MAIN CPU reads data from the ROM and the RAMs. |
| 45 | $\overline{W R}$ | OUT | Write signal. Drops to " L " when MAIN CPU writes data into the RAMs. |
| 46 | ALE | OUT | Address Latch Enable. When " H ", data bus D0 ~ D7 becomes address bus A0~A7. |
| $47 \sim 54$ | PFO(A8) ~PF7(A15) | OUT | Upper address bus ( $\mathrm{A} 8 \sim \mathrm{~A} 15$ ) |
| $55 \sim 62$ | PD0(D0) ~PD7(D7) | IN/OUT | Data bus (D0~D7) |
| 63, 64 | VDD, VCC | IN | +5 V power source |

8. SUB-CPU ( $\mu$ PD7811-204)

| PIN NO. | TERMINAL NAME | IN/OUT | FUNCTION |
| :---: | :---: | :---: | :--- |
| $1 \sim 8$ | PAO(LO)~PA7(L7) | OUT | LED drive signals |
| 9 | PB0 | IN | Data receive request from Master Music LSI |
| 10 | PB1 | IN | Data receive request from Slave Music LSI |
| 11 | PB2 | OUT | Master Music LSI chip select signal |
| 12 | PB3 | OUT | Slave Music LSI chip select signal |
| 13 | PB4 | OUT | Write enable signal for Music LSIs |
| 14 | PB5 | OUT | ID (Interrupt Disable) signal. <br> When SUB-CPU is busy, it sends ID signal to <br> Music LSIs so as not to be interrupted. |
| 15 | PB6 (LDC) | OUT | Stays "H" level for approximately 830 milli- <br> seconds after the power switch is turned on in <br> order to avoid mis-lighting the LEDs at Power <br> ON. |
| 17 | PC0 (TXD, L11) | OUT | LED drive signal |
| 18 | PC1 (RXD, SYNC) | IN | Synchronous signal from MAIN CPU |
| 19 | PC2 (SCK, CONT) | IN/OUT | Control signal between MAIN and SUB-CPUs |
| 20 | PC3 (INT2) | IN | Interrupt signal from Music LSIs <br> 21 |
| PC4 (T0) | OUT | Metronome envelope signal |  |
| $22 \sim 24$ | PC5(L8)~PC7 (L10) | OUT | LED drive signals <br> 26 |
| INT1 | IN | Interrupt signal from MAIN CPU |  |


| 28 | $\overline{\text { RESET }}$ | IN | At Power ON, the terminal stays " $L$ " level for a while in order to initialize the internal circuits. |
| :---: | :---: | :---: | :---: |
| 31 | X1 | IN | 12 MHz clock pulse |
| 32 | VSS | IN | Ground ( 0 V ) power source |
| 44 | $\overline{\mathrm{RD}}$ | OUT | Read signal. Drops to "L" when SUB-CPU reads data from the ROM, RAMs or Music LSIs. |
| 45 | $\overline{W R}$ | OUT | Write signal. Drops to "L" when SUB-CPU writes data into the RAMs or Music LSIs. |
| 46 | ALE | OUT | Address Latch Enable. <br> When " H ", data bus PD9 (DS0) ~ PD7 (DS7) becomes address bus AS0 ~ AS7. |
| 47~54 | PFO(AS15) <br> ~ PF7 (AS8) | OUT | Upper address bus |
| 55~62 | PDO(DSO) <br> ~ PD7 (DS7) | OUT | Data bus |
| 63,64 | VDD, VCC | IN | +5 V power source |



The first 2 K bytes of Main RAM 1 are the data area for system execution and the rest of 6 K bytes and the whole 8 K bytes of Main RAM 2 are the data area for programmed music.
The capacity of Main ROM is 32 K bytes and contains the program for system execution.
The lower address bus AO ~ A7 is provided from CPU Interface LSI. When signal ALE from MAIN CPU rises to " H ", data bus (D0 ~ D7) becomes address bus (A0 ~ A7) in CPU Interface LSI. The upper address A8 ~ A15 is directly supplied from MAIN CPU.

Chip select signals are provided from signals A13 ~ A15:

| A13 | A14 | A5 |  |
| :---: | :---: | :---: | :--- |
| L | L | H | Main RAM 1 chip selection |
| H | L | L | Main RAM2 chip selection |
| X | X | L | Main ROM chip selection |

'LS138, 'S138 FUNCTION TABLE

| INPUT |  |  |  |  | OUTPUT |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ENABLE |  | SELECT |  |  |  |  |  |  |  |  |  |  |
| G1 | G2*. | C | B | A | YO | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | $\times$ | $\times$ | X | H | H | H | H | H | H | H | H |
| L | X | $\times$ | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L |  | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L. | H | H | L | H | H | H | H | H |
| H | L |  | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L |  | L |  | H | H | H | H | H | L | H | H |
| H | L |  | H |  | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

[^0]

TC5516AP is a 2 K -byte RAM while HN61364P is an 8K-byte ROM.
Sub-RAM 1 - Tone data area for Memory Banks A and B.
Sub-RAM 2 - Data area for system execution.
Sub-RAM 3 - Tone data area for Memory Banks C and D.

In the same procedures as for MAIN CPU, lower address bus ASO ~ AS7 is generated from data bus DSO ~ DS7 in CPU Interface LSI when signal ALE is " $H$ ". Upper address signals A8 ~ A15 are provided from SUB-CPU directly.
Decoder 74LS138-2 generates chip selection signals and other control signals from signals AS11 ~AS15 as follows:

| 74LS138 | 74LS138 |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | IN |  |  |  |  | OUT |  |  |  |  |  |  |  |  |
|  | A14 | A15 | A13 | A12 | A11 | YO | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |  |
| A15-G1 YO | L | H | L | L | L | L | H | H | H | H | H | H | H | Write strobe for Music LSIs |
| A14-G2 Y1 | L | H | L | L | H | H | L | H | H | H | H | H | H | Data transfer: SUB-CPU $\rightarrow$ MAIN CPU |
| $\overline{\mathrm{RD}} \cdot \overline{\mathrm{WR}}-\mathrm{G} 2 \mathrm{~B} \quad \mathrm{Y} 2$ | L | H | L | H | L | H | H | L | H | H | H | H | H | Data transfer: MAIN CPU $\rightarrow$ SUB-CPU |
| $A 11-A \quad Y 3$ | L. | H | L | H | H | H | H | H | L | H | H | H | H | Data transfer: MAIN CPU $\rightarrow$ SUB-CPU |
| A12-B Y4 | L | H | H | L | L | H | H | H | H | L | H | H | H | MAIN CPU interruption |
| A13-C Y5 | L | H | H | L | H | H | H | H | H | H | L | H | H | Sub-RAM 2 chip selection |
| Y6 | L | H | H | H | L | H | H | H | H | H | H | L | H | Sub-RAM 1 chip selection |
| Y7 | L | H | H | H | H | H | H | H | H | H | H | H | L | Sub-RAM3 chip selection |

## 11. MUSIC LSIS ACCESS

CZ-5000 employs two Music LSIs, Master LSI and Slave LSI, which are controlled by SUB-CPU.


SUB CPU $\Rightarrow$ Music LSI


1) Music LSI $\Rightarrow$ SUB-CPU


Upon receipt of an interrupt signal,

12. CPU INTERFACE (MB64H173)


Internal block diagram of MB64H173

F/F 1 - Set by the clock pulse '0' and signal R2 from SUB-CPU, and generates signal SYNC which synchronizes MAIN and SUB-CPUs.

FUNCTION TABLE

| INPUT |  |  |  |  | OUTPUT |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PRESET | CLEAR | CLOCK | D | Q | $\overline{\mathrm{Q}}$ |  |
| L | H | X | X | H | L |  |
| H | L | $\times$ | $\times$ | L | H |  |
| L | L | $\times$ | $\times$ | $H^{*}$ | $\mathrm{H}^{*}$ |  |
| $H$ | $H$ | $\uparrow$ | $H$ | $H$ | L |  |
| $H$ | $H$ | $\uparrow$ | L | L | $H$ |  |
| $H$ | $H$ | L | $\times$ | $\mathrm{Q}_{0}$ | $\overline{\mathrm{Q}}_{0}$ |  |

Decoder 1 - Generates clock pulses for the latches from signals A0~A3, A14, A15, $\overline{R D}$ and $\overline{W R}$.

FUNCTION TABLE

| ENABLE INPUT |  | SELECT INPUT |  |  | OUTPUT |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| G1 | $\overline{\mathrm{G}} 2^{*}$ | C | B | A | YO | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| $\times$ | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L. | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

$* \overline{\mathrm{G}} 2=\overline{\mathrm{G}} 2 \mathrm{~A}+\overline{\mathrm{G}} 2 \mathrm{~B}$

Latch 1 - Converts MAIN CPU's data bus (D0 ~ D7) into address bus A0 ~ A7, and generates clock pulses ' 0 ' ~ ' 5 '.

Latch 2 - For the data transfer from MAIN CPU to SUB-CPU.
Latch 3 - Transfers the data from the pitch bender and modulator wheel to SUB-CPU.
Latch 4 - For the data transfer from SUB-CPU to MAIN CPU.
Latch 5 - Converts SUB-CPU's data bus (DS0 ~ DS7) into address bus ASO ~ AS7.
FUNCTION TABLE

|  | INPACH | LATCH) |  |
| :---: | :---: | :---: | :---: |
| $\overline{O C}$ | ENABLE C | $D$ | OUTPUT |
| $L$ | $H$ | $H$ | $Q$ |
| $L$ | $H$ | $L$ | $H$ |
| $L$ | $L$ | $X$ | $L$ |
| $H$ | $X$ | $X$ | $Q_{0}$ |

Latch 1 and 5

FUNCTION TABLE (EACH FLIP-FLOP)

| INPUT |  |  | OUTPUT |
| :---: | :---: | :---: | :---: |
| $\overline{\mathrm{OC}}$ | CLK | D | Q |
| $L$ | $\uparrow$ | $H$ | H |
| L | $\uparrow$ | L | L |
| L | L | $\times$ | $\mathrm{Q}_{0}$ |
| $H$ | $X$ | $\times$ | $Z$ |

Latch $2 \sim 4$

12-2. Data Transfer Procedures

(1) Pitch Bender \& Modulator $\square$ SUB-CPU.
(1) Voltage level from the pitch bender or the modulator is converted into digital data in the CPU's builtin ADC (Analog to Digital Converter) and output from data bus (D0 ~ D7).
(2) The data is entered into CPU Interface LSI.
(3) Sending signal R1, SUB-CPU sets Latch 3 and reads data periodically.
(2) MAIN CPU $\square$ SUB-CPU.
(1) Via Latch 1 and Decoder 1, MAIN CPU drops clock pulse ' 0 ' to " $L$ " level. By clock pulse ' 0 ', F/F 1 is preset to rise signal SYNC.
(2) MAIN CPU puts data on data bus DO ~ D7, and at the same time, clock pulse ' 0 ' rises to " H " level.
At the rising edge of clock pulse ' 0 ', data from MAIN CPU is set in Latch 2.
(3) MAIN CPU interrupts SUB-CPU from terminal PB2, and simultaneously generates signal CONT from terminal PB3.
(4.) Generating signal R2 from Decoder 3, SUB-CPU reads the data from Latch 2 via data bus DSO ~ DS7.
(5) SUB-CPU sends signal ACK to MAIN CPU via Decoder 3 and F/F 2.

Upon receipt of signal ACK, MAIN CPU confirms that SUB-CPU has received the data and generates signal $\phi 16$ in Decoder 2.
(6) When all the data have sent to SUB-CPU by repeating the above procedures (1)~ (5), MAIN CPU drops signal CONT to " $L$ ".
(7) Confirming that both CONT and SYNC are "L", SUB-CPU determines that all the data have been received.

(3) Sub-CPU $\underset{\square}{\square}$ MAIN CPU.
(1) In the same procedures as stated in the item (2), MAIN CPU sends "Request Command" that inquires SUB-CPU to transmit data.
(2) SUB-CPU puts data on the data bus DSO ~ DS7 and sets the data in Latch 4 by signal W1. SUB-CPU then presets F/F 2 by pulse $\phi 4$, causing signal ACK to be entered in MAIN CPU.
(3) Acknowledging that the data is set in Latch 4 by signal ACK, MAIN CPU generates clock pulse '2', causing the data from SUB-CPU to be put on MAIN CPU data bus D0 ~ D7.
(4) After receiving the data, MAIN CPU sends SUB-CPU an interrupt signal from terminal PB2, and by the interrupt signal, SUB-CPU confirms that the data is received by MAIN CPU.
(5) Repeating the above procedures (2) ~ (4), SUB-CPU sends the next data to MAIN CPU.

(4) Key and switch scanning

Receiving a key common signal from data bus, MAIN CPU discriminates a key or a switch input.

(1) From signals PAO ~ PA3 of MAIN CPU, 4-line to 16 -line decoder 74LS154P-1 generates key common signals $\mathrm{KCO} \sim \mathrm{KC14}$.
(2) When a key or a switch is hit, one of the input signals KIO~KI5 (for keys) or KI10 ~ KI15 (for switches) is entered in CPU Interface MB64H173.
(3) MAIN CPU generates the clock pulse '3' (for keys) or '4' (for switches), causing the tristate buffers to be opened.
(4) The input pulse is entered into data bus.
(5) Discriminating the contents of the data bus, MAIN CPU determines which key is hit.

| INPUT |  |  |  |  |  | OUTPUT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| G1 | G2 | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H . | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | $L$ | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | $L$ | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| $L$ | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | X | X | X | $\times$ | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | x | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | $\times$ | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |


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| $\begin{gathered} 乙 \\ \times \forall \forall \forall \perp \end{gathered}$ | ત્ર૭૪ப1 | $\exists$ WIL 7 $\forall \exists$ y <br>  | $7 \forall \cap N \forall W$ <br>  | वч03ヨy | คヨSヨy |  |  |  |  |  | 10 | OLכX |
| $\begin{gathered} 8 \\ \text { அ્ヤソ1 } \end{gathered}$ | $\begin{gathered} L \\ \times \forall \forall \cup \perp \end{gathered}$ |  | G <br>  | $\begin{gathered} \stackrel{\nabla}{x} \\ \times 10 \forall y \perp \end{gathered}$ | $\begin{gathered} \varepsilon \\ \underset{y}{\varepsilon} \forall \cup \perp \end{gathered}$ | 98 | 9\＃$\forall$ | $9 \forall$ | 9\＃9 | 99 | 9\＃」 | 6 Јヤ |
| $\exists \mathrm{N} \cap \perp \mathrm{Bl}$ | ヨ1ヨาヨロ | NMOO OdWヨ」 | dn OdWヨ1 | $1 \forall \exists d \exists \underline{y}$ | ત્રЭヨНЭ ત્રכヤソ1 | $9 \pm$ | $9 \exists$ | 9\＃0 | 90 | 9\＃つ | 93 | 8 Јヤ |
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| $\wedge N \exists$ <br> $1 \forall 00$ | $\begin{aligned} & \text { む人ヨ지 } \\ & \quad 1 \forall 00 \end{aligned}$ | $\wedge \mathrm{N} \mathrm{\exists}$ 1 MOC | $\begin{aligned} & \pm \times \wedge \exists> \\ & \quad 1 \text { MOa } \end{aligned}$ | $\wedge N \exists$ <br> 1000 | WとO－コ $\wedge \forall M$ <br> 1000 | Gy | Gヨ | 9\＃O | GO | ¢\＃О | 93 | 9 Ј入 |
| $\exists \mathrm{SION}$ | ONIC |  |  | $\exists \wedge \forall \perp$ O | $\exists \mathrm{I}$ I $\forall 1 \perp$ INI | t8 | $t \# \forall$ | $\forall \forall$ | も\＃ | $\dagger \bigcirc$ | 囲」 | ¢ コ＞ |
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| t $\exists \mathrm{NO} \perp$ | $\begin{gathered} \varepsilon \\ \exists N O \perp \end{gathered}$ | $\begin{gathered} \text { 乙 } \\ \exists N O \perp \end{gathered}$ | $\stackrel{\llcorner }{\exists \mathrm{NO} \perp}$ | $\begin{aligned} & \text { Sヨ人 } \\ & \text { yOSU@ } \end{aligned}$ | $\begin{aligned} & \text { ON } \\ & \text { yOSy o } \end{aligned}$ | £コ | £ヨ | £\＃О | $\varepsilon \square$ | £\＃つ | ยว | 乙 Ј入 |
| $\begin{aligned} & g \cdot \gg N \forall G \\ & \quad \perp \exists S \exists y d \end{aligned}$ | $\begin{aligned} & \forall->N \forall G \\ & \quad \perp \exists \mathrm{~S} \mathrm{\exists} \text { yd } \end{aligned}$ | $\begin{gathered} 8 \\ \exists \mathrm{NO} \perp \end{gathered}$ | $\underset{\exists N O \perp}{L}$ | $\begin{gathered} 9 \\ \exists \mathrm{NO} \perp \end{gathered}$ | $\begin{gathered} \mathrm{G} \\ \exists \mathrm{NO} \perp \end{gathered}$ | 28 | て\＃$\forall$ | てV | て\＃け | 乙Э | て\＃」 | L O＞ |
| व•ㄱN $\forall 8$入YOWヨW | う－＞ <br> 人 $40 W \exists$ W | $g \cdot>1 N \forall 8$ 드NW | $\forall$－$>1 N \forall 8$ LヨSヨyd | $\begin{aligned} & a \cdot \times \times N \forall G \\ & \quad \perp \exists S \exists y d \end{aligned}$ |  | てJ | $2 \exists$ | て\＃0 | て○ | て\＃つ | Z） | 0 Ј入 |
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## 14. LED DRIVING CIRCUITS

74LS174
FUNCTION TABLE
(EACH FLIP-FLOP)

| INPUT |  |  | OUTPUT |  |
| :---: | :---: | :---: | :---: | :---: |
| CLEAR | CLOCK | D | Q | $\overline{\mathrm{Q}} \uparrow$ |
| L | $\times$ | $\times$ | L | $H$ |
| $H$ | $\uparrow$ | $H$ | $H$ | L |
| $H$ | $\uparrow$ | $L$ | L | $H$ |
| $H$ | $L$ | $X$ | $Q_{0}$ | $\mathrm{Q}_{0}$ |

74LS154P
FUNCTION TABLE
$H=$ high level (steady state)
$\mathrm{L}=$ low level (steady state)
$X=$ irrelevant
$\uparrow=$ transition from low to high level
$\mathrm{Q}_{0}=$ the level of Q before the indicated steady-state input conditions were established.

|  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |


| $1 / G 2$ | $D$ | $C$ | $B$ | $A$ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 14 | 15 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | . L L L L L L H H H H H H H H H H H H H H H L L L L H $\quad H \quad L \quad H \quad H \quad H \quad H \quad H \quad H \quad H \quad H \quad H \quad H \quad H \quad H \quad H \quad H$ $\begin{array}{lllllllllllllllllll}L & L & L & H & L & H & H & L & H & H & H & H & H & H & H & H & H & H & H \\ H & H \\ L & L & L & H & H & H & H & H & L & H & H & H & H & H & H & H & H & H & H\end{array}$ $\begin{array}{lllllllllllllllllll}L & L & H & H & H & H & H & L & H & H & H & H & H & H & H & H & H & H & H\end{array}$


 $\begin{array}{lllllllllllllllllll}L & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H & H & H & H\end{array}$ H Llllllllllllllllll $\begin{array}{lllllllllllllllllll}H & L & L & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H & H \\ H\end{array}$ $H L H H$
$\qquad$ H H L H H H H H H H
$\begin{array}{llll}\mathrm{H} & \mathrm{H} & \mathrm{H} & \mathrm{L} \\ \mathrm{H} & \mathrm{H}\end{array}$
H H H H
$\times \times \times \times H$
$\begin{array}{llllllllllllllllll}L & X & X & X & X & H & H & H & H & H & H & H & H & H & H & H & H & H\end{array} H$
high level, $L=$ low level, $X=$ irrelevant


Combining the signals $A 0 \sim A 3$, Decoder 4 generates signals $\phi 17 \sim \phi 19$ and $\phi 1 A \sim$ $\phi 1 \mathrm{D}$ which set Latches $5 \sim 11$.
For lighting the LED "NORMAL", MAIN CPU raises signal DO which is inverted to "L" level.

Then, MAIN CPU generates clock signal $\phi 17$ from signals $A 0 \sim A 3$.
$\overline{\mathrm{DO}}\left(=\right.$ " $\left.L^{\prime \prime}\right)$ is set in Latch 5 dropping signal L70 "L".
The LED "NORMAL" is lit when its anode is connected to VDL2 $(+5 \mathrm{~V})$.

Signal Conditions


These LEDs are controlled by SUB-CPU.
For example, when SUB-CPU wishes to light the "PRESET BANK-A" LED, it drops all the signals L8 ~ L11. Y0 output of Decoder 5 drops to " $L$ ", causing the LED to be lit.
15. ANALOG CIRCUIT BLOCK DIAGRAM


Master and Slave Music LSIs provide 12-bit digital sounds for DAC (Digital to Analog Converter). By means of time sharing, DAC mixes the two different signals and converts into analog waveforms. To obtain a wide dynamic range of the amplitude, Music LSIs' outputs are contracted and are reformed into a proper waveform shape by Expander circuits. Sample \& Hold circuit removes a high frequency noise called as glitch contained in the DAC output.
Sample \& Hold Circuit also separates the Master and Slave waveforms.
16. MUSIC LSI ( $\mu$ PD933)

| PIN NO. | TERMINAL NAME | IN/OUT | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1~8 | DB7 ~ DB0 | IN/OUT | 8 -bit data bus between Music LSIs and SUB-CPU |
| 9 | $\overline{C S}$ | IN | Chip select terminal. At " $L$ ", the LSI is designated by SUB-CPU. |
| 10 | $\overline{\mathrm{RD}}$ | IN | Read data terminal. At " $L$ ", the $L S I$ sends data to SUB-CPU. |
| 11 | $\overline{W E}$ | IN | Write enable terminal. At "L", the LSI receives data from SUB-CPU. |
| 12 | $\overline{W S}$ | IN | Write strobe terminal. SUB-CPU writes data into Music LSI at the rising edge of the signal. |
| 16 | M/S | IN | Master or Slave determination terminal. When "L", the LSI becomes Slave LSI while it becomes Master LSI when the terminal is " H ". |
| 17 | SYC | IN/OUT | Synchronous signal input/output terminal. The synchronous signal is sent from Master LSI to Slave LSI. |
| 18 | CLK | IN | 4.48 MHz clock pulse input |
| 21 | RST | IN | Reset signal input. Normally the terminal stays "L". At power ON, the terminal rises to " H " level for a while and the internal circuits of the LSI are initialized. |
| 22 | DOE | IN/OUT | Data output enable terminal. At " H ", digital sound signals are output from Master LSI while Slave LSI outputs sound signal at "L" level. |
| 23 | SH | OUT | 40 KHz sampling signal for Sample \& Hold circuit |
| 25~27 | DO1 ~ DO3 | OUT | Control signals for Expander circuit |
| $28 \sim 39$ | DO4 ~ DO15 | OUT | 12-bit digital sound signals |
| 40 | VDD | IN | +5 V power source |

## 17. DAC (Digital to Analog Converter)

The two Music LSIs output different waveforms. When signal DOE is " $H$ ", Master LSI outputs a waveform while Slave LSI outputs a waveform at "L" level of DOE.


## 18. EXPANDER CIRCUIT

In order to extend the dynamic range of the melody signal, a part of DAC output waveform is contracted and expanded by Expander Circuit.


In accordance with the voltage levels of the signals DO1, DO2 and DO3, one of the input channels is turned on.
By the resistors connected to each channel, the amplitude of DAC output varies from 1 to 1/16.


Combined resistances at each point are:
$\mathrm{ra}=\mathrm{R} 1(5 \mathrm{~K} \Omega)+\mathrm{R} 2(5 \mathrm{~K} \Omega)=10 \mathrm{~K} \Omega$
$\mathrm{rb}=$ Parallel connected ra $(10 \mathrm{~K} \Omega)$ and $\mathrm{R} 3(10 \mathrm{~K} \Omega)=5 \mathrm{~K} \Omega$
$\mathrm{rc}=\mathrm{rb}(5 \mathrm{~K} \Omega)+\mathrm{R} 4(5 \mathrm{~K} \Omega)=10 \mathrm{~K} \Omega$
$r d=$ Parallel connected rc $(10 \mathrm{~K} \Omega)$ and $\mathrm{R} 5(10 \mathrm{~K} \Omega)=5 \mathrm{~K} \Omega$
$r e=r d(5 K \Omega)+R 6(5 K \Omega)=10 \mathrm{~K} \Omega$
rf $=$ Parallel connected re $(10 \mathrm{~K} \Omega)$ and $\mathrm{R} 7(10 \mathrm{~K} \Omega)=5 \mathrm{~K} \Omega$
$r g=r f(5 K \Omega)+R 8(5 K \Omega)=10 K \Omega$

Each current value is:
$1=111+112$
$111=121+122$
$121=131+132$
Namely, $111=1 / 2$

$$
\begin{aligned}
& I 21=111 / 2=1 / 4 \\
& I 31=121 / 2=1 / 8
\end{aligned}
$$

Voltage level at each channel is:
Channel 0: $\mathrm{rg} \times \mathrm{I}=10 \mathrm{~K} \Omega \times \mathrm{I}$
Channel 1: re $\times 111=10 \mathrm{~K} \Omega \times 1 / 2$
Channel 2: $r c \times 121=10 \mathrm{~K} \Omega \times \mathrm{I} / 4$
Channel 3: $\operatorname{rax} \mathrm{I} 31=10 \mathrm{~K} \Omega \times \mathrm{I} / 8$
Channel 4: $\mathrm{R} 1 \times \mathrm{I} 31=5 \mathrm{~K} \Omega \times \mathrm{I} / 8=10 \mathrm{~K} \times \mathrm{I} / 16$

If input voltage is $E$ :
Channel 0 input voltage is $E$.
Channel 1 input voltage is $E / 2$.
Channel 2 input voltage is $E / 4$.
Channel 3 input voltage is $E / 8$.
Channel 4 input voltage is $E / 16$.

Thus, output of DAC is expanded in accordance with the voltage levels of signals DO1, DO2 and DO3.
19. SAMPLE \& HOLD CIRCUIT


The block eliminates a high frequency noise called as "Glitch" which appears at the end of the stepped waveform.


When signal SH from Master LSI is " H ", the switch X in TC4053 is contacted with the terminal $O X$. This causes the input signal to pass through. At this time, the voltage level of the waveform is charged in the Hold Capacitor.
On the other hand, while a glitch appears on the waveform, the switch $X$ is contacted with the terminal IX. This results in cutting off the glitch. Although no signal comes out of TC4053, the input of the opamp keeps the same voltage level by discharging of the Hold Capacitor.
Sampling or holding the slave waveform is performed by the same procedures using signal SH from Slave LSI and switch Z.

## 20. STEREO CHORUS CIRCUIT



Function of Each Block:
Filter A - Smoothes the stepped waveform of Samle \& Hold Circuit output signal.
Filter B - As the BBD does not pass signals which exceed 20 KHz , this block is a low-pass filter whose cutoff frequency is 20 KHz .

Compressor - In accordance with input signal level, this block controls the amplitude. When the input signal is small, the circuit amplifies the signal whereas the amplitude becomes smaller when the input is a large-level waveform. The block is used for reducing the noise.

Three-Phase LFOs - Generates low-frequency triangle signals of 0.54 Hz and 6.1 Hz . The three outputs differ 120 degrees in phase.

VCOs - Voltage Controlled Oscillator which generates the clock pulses for the BBDs. Their oscillation frequencies vary in accordance with the input voltage level.

BBDs

Filter C

Expander

- Functions contrary to the Compressor. This circuit is also used for reducing the noise.


## 20-1. Three-Phase LFO (Low Frequency Oscillator)



The left figure shows three inverters serially connected. If " L " level input enters the circuit, the output becomes " H " level. Because of the transfer characteristic of the inverter, the inverted input voltage appears on the output with a time lag. Hence, the circuit oscillates and the oscillation frequency is determined by the time lag.

The following shows the actual circuit of the Three-Phase LFO. The time lag is controlled by the parallel connected capacitor and the resistors.
Model CZ-5000 employs two LFOs whose oscillation frequencies are 0.54 Hz and 6.1 Hz . The output differs 120 degrees in phase.


Both 0.54 Hz and 6.1 Hz triangle waveforms are mixed to give variational delays of the sound in the BBD.


The 0.54 Hz and 6.1 Hz waveforms are mixed in the ratio of $10: 1$ as they pass through 18 Kohm and 180 Kohm resistors, respectively.

20-2. VCO (Voltage Controlled Oscillator)






The VCO is an oscillator whose oscillation frequency varies in accordance with the input voltage level.

In the left figure, the voltage levels of the A-OUT and the B-OUT are opposite.
(1) When A-OUT is " $H$ ", B-OUT drops to " $L$ ".
(2) From A-OUT, electric current flows into B-IN via a differentiation circuit.
As a result, the voltage of B-IN drops gradually while the $\mathrm{A}-\mathrm{IN}$ voltage gradually rises.

(3) When B-IN becomes lower than the threshold level, B-OUT rises to " H ".
When A-IN becomes higher than the threshold level, A-OUT drops to "L".
(4) The circuit oscillates repeating the above operations.

The following shows the actual circuit of VCO. When control terminal (A) is GND (zero volt), it takes approximately 15 microseconds for the differentiation circuit to reach the threshold voltage.


When the voltage of (A) is 2 volts, it takes only 9 microseconds to reach the threshold level.


As VCO receives a triangle waveform from the Three-Phase LFO, it oscillates from 55.6 KHz to 33.3 KHz in accordance with the voltage level of LFO output.

## 20-3. BBD (Bucket Brigade Device)



The BBD contains serial-connected delay elements. The input signal is shifted one step per one clock pulse.
The clock pulse is generated in the VCO , and as it varies from 33.3 KHz to 55.6 KHz , the delay time varies.


Model CZ-5000 employs three BBDs in order to give better stereo effect.

### 20.4. Compressor and Expander Circuits

If a sound signal passes through the BBD, a noise is carried on the signal especially when the input level of the signal is low.


Compressor When the level of input signal is low, the amplitude is large. If the input level is high, the amplitude decreases.


Expander
When the level of input signla is low, the amplitude is small. The amplitude increases when the input level is high.


When a low signal does not pass through the Compressor and the Expander;


When a low signal passes through the Compressor and the Expander;


Thus, the $\mathrm{S} / \mathrm{N}$ ratio of the circuit is heightened.

## 21. VOLUME CONTROL CIRCUIT



Electric current from pedal and main volume controls are amplified by transistors T 4 and T 3 , respectively, and become the base current of transistor T2. Collector current of T2 is applied to NJM13600's control terminals.
NJM13600 is a power amplifier with control terminals.
In accordance with the amount of the current applied to pins 1 and 16, the amplitude of the amplifier varies.
22. RESET CIRCUIT


## 23. MIDI \& MT INTERFACE CIRCUITS

## 23-1. MIDI Interface Circuit

MIDI (Musical Instrument Digital Interface) is an international standard for the external control of electronic musical instruments. In other words, standardized input and output terminals are equipped with musical instruments, rhythm machines, sequencers, etc. and the music information which the machines send and receive via these terminals is made compatible by certain formatting This standard enables a musical instrument to connect, synchronize, and sequence (memorize) to other models and even to other brands.


Serial data information from other instruments comes in from the MIDI-IN terminal and enters into MAIN CPU's PC1 terminal via photo coupler PC900. The CZ-5000 is not thus electrically connected with any external instruments; which causes electric noises to be cut off. MAIN CPU transmits MIDI data from PCO terminal.


Digital data of 1 and 0 are recorded on magnetic tape as 2.4 KHz and 1.2 KHz sound, respectively.
When data is read, a signal from a cassette tape player comes in from MT terminal pin 5 .
As the voltage level varies depending on cassette tape players, the two zener diodes cramp the signal between 0 and +5 volts.
The cramped waveform is amplified by the first opamp. The second stage opamp is a comparator which examines whether the input voltage is higher or lower than 2.5 V and outputs a square waveform to MAIN CPU's PC3 terminal.
As 5 volts of MAIN CPU's PB1 terminal is too high for a cassette tape recorder, it is dropped to 34 millivolts by the 100 Kohm and 680 ohm resistors.
Signal PB4 from MAIN CPU turns on and off the remote control relay which controls the motor in a cassette tape player.
24. ADJUSTMENT

## 24-1. DAC Offset Voltage


(1) Connect a digital voltmeter between pin 13 or 19 of DAC BA9221 and pin 7 of opamp TL082-3.
(2) While the test unit is not producing any sound, adjust VR2 on PCB M5153-MA1M so that the voltmeter reading is $0 \pm 3 \mathrm{mV}$.

## 24-2. Volume Adjustment

(1) Keep pressing "INITIALIZE" button, depress "DC01 WAVEFORM", "DC01 ENVELOPE", "DCW1 KEY FOLLOW", DCW1 ENVELOPE", DCA1 KEY FOLLOW" and "DCA1 ENVELOPE" buttons.
(2) Depress "DCW1 ENVELOPE" and then "END" buttons.
(3) Choose $1+1$ ' by "LINE SELECT" button.
(4) Set the volume control to its maximum and the stereo chorus volume to its minimum.
(5) Connect a digital voltmeter between the ground and LINE-OUT terminal (either left or right output).
(6) Depressing a key, adjust 50K VR on the PCB M5153-AS1M so that the voltmeter reading is 360 mV ( 510 mV when an oscilloscope is used for checking the voltage).

## PARTS LIST

## MPL. 042

CZ-5000 (MX-153)

Note: 1. Prices and specifications are subject to change without notice.
2. As for spare parts order/supply, refer to the separate publication, "GUIDEBOOK for Spare Parts Supply".

| Item | Code No． | Part Name | Specification | Q＇ty | ＊ | Unit Price J．F．Yen（ $¥$ ） （FOB：JAPAN） | R A N K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 1）MA1M PCB ASS＇Y |  |  |  |  |  |
| 4 | 20010525 | C－MOSIC | MB64H173 | 1 |  |  | A |
| $\pi$ | 20011092 | LSI | HN61364P－E39 | 1 |  |  | A |
|  | 20020971 | LSI | $\mu$ PD933D | 2 |  |  | A |
| 白 | 20021128 | LSI | $\mu \mathrm{PD} 7811 \mathrm{G}-180$ | 1 |  |  | A |
| \％ | 20021136 | LSI | $\mu \mathrm{PD} 7811 \mathrm{G}-204$ | 1 |  |  | A |
| 5 | 20091235 | LSI | HM6264LP－15 | 2 |  |  |  |
|  | 21003808 | C－MOSIC | TC4053BP | 1 |  |  | A |
|  | 21003841 | LSI（RAM） | TC5516AP | 3 |  |  | A |
|  | 21004029 | C－MOSIC | TC4051BP | 1 |  |  | A |
|  | 21004472 | C－MOSIC | TC74HCU04P | 2 |  |  | A |
| 4 | 21004642 | C－MOSIC | TC53257P－1255 | 1 |  |  |  |
|  | 21103756 | IC | SN74LS04N | 1 |  |  | A |
|  | 21112178 | IC | SN74LS74AN | 2 |  |  | A |
|  | 21112194 | IC | SN74LS138N | 2 |  |  | A |
|  | 21112283 | IC | SN74LS08N | 1 |  |  | A |
|  | 21112496 | IC | SN74LS174N | 2 |  |  | A |
|  | 21112615 | IC | SN74LS05N | 1 |  |  | A |
| ［s | 21209341 | IC | TL082 | 3 |  |  | A |
| 立 | 21220221 | D／A converter | BA9221 | 1 |  |  | A |
|  | 21841014 | IC | HD74LS154P | 2 |  |  | A |
|  | 25203194 | Crystal oscilator | HC－18／U－8960kHz | 1 | 10 |  | B |
| \％ | 25203224 | Crystal oscillator | HC－18／U－12MHz | 1 | 10 |  | B |
|  | 27202519 | Module resistor | MS3329 | 1 | 10 |  | C |
|  | 27202811 | Module resistor | MS4736 | 2 | 10 |  | C |
|  | 27202837 | Module resistor | MS3326 | 1 | 10 |  | C |
|  | 27602177 | Trimmer VR | V8K4－11B10K | 1 | 10 |  | B |
| \％ | 27602258 | Trimmer VR | V8K4－118200 | 1 | 10 |  | B |
| $s$ | 28056273 | Electrolytic capacitor | SMC6．3VB－470（M） | 1 | 10 |  | C |
|  | 35003371 | Connector 2P | IL－G－2P－S3T2－E | 2 | 10 |  | $\times$ |
|  | 35003428 | Connector 9P | IL－G－9P－S3T2－E | 2 | 10 |  | $x$ |
|  | 35007032 | P．C．board connector | 5229－13－CPB | 1 | 10 |  | $x$ |
|  | 35007041 | P．C．board connector | 5229－17－CPB | 1 | 10 |  | $x$ |
| 宜 | 35007059 | P．C．board connector | 5229－23－CPB | 1 | 10 |  | $x$ |
|  | 35007491 | P．C．board connector | IL－G－14P－S3T2－E | 1 | 10 |  | $x$ |
|  | 35007505 | P．C．board connector | IL－G－6P－S3T2－E | 2 | 10 |  | $x$ |
| 古 | 35008169 | P．C．board connector | ZC－026 | 1 | 10 |  | $x$ |

Note： －New part
Q＇ty－Quantity used per unit
＊－Minimum order／supply quantity

Rank A ：Essential
B ：Stock recommended
C ：Others
X ：No stock recommended

| Item | Code No. | Part Name | Specification | Q'ty | * | Unit Price J.F. Yen ( $¥$ ) (FOB: JAPAN) | R A N K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \% | 35110933 | P.C. board connector | 5229-12CPB | 1 | 10 |  | x |
|  | 37307301 | Parallel wire M153 | 2468-7-230 | 1 | 10 |  | X |
|  | 22003721 | Transistor | 2SA933-SQ | 5 | 10 |  | B |
|  | 22201395 | Transistor | 2SC1740SQ | 6 | 10 |  | B |
|  | 23013002 | Diode | DS-442 | 6 | 10 |  | C |
|  | 23103265 | Zener diode | RD5.6E(B2) | 1 | 10 |  | B |
|  | 23103338 | Zener diode | RD3.3E(B2) | 1 | 10 |  | B |
|  | 26007313 | Carbon film resistor | R-25-10K-J | 10 | 10 |  | C |
|  | 26009715 | Carbon film resistor | R-25-100K-J | 1 | 10 |  | C |
|  | 26007712 | Carbon film resistor | R-25-15K.J | 3 | 10 |  | C |
|  | 26005515 | Carbon film resistor | R-25-1.8K-J | 1 | 10 |  | C |
|  | 26010918 | Carbon film resistor | R-25-330K-J | 1 | 10 |  | C |
|  | 26006716 | Carbon film resistor | R-25-5.6K-J | 4 | 10 |  | C |
|  | 26006911 | Carbon film resistor | R-25-6.8K-J | 5 | 10 |  | C |
|  | 26002516 | Carbon film resistor | R-25-100-J | 2 | 10 |  | C |
|  | 26003717 | Carbon film resistor | R-25-330-J | 1 | 10 |  | C |
|  | 26004314 | Carbon film resistor | R-25-560-J | 2 | 10 |  | C |
|  | 26004918 | Carbon film resistor | R-25-1K-J | 90 | 10 |  | C |
|  | 26012112 | Carbon film resistor | R-25-1M-J | 3 | 10 |  | C |
|  | 26005710 | Carbon film resistor | R-25-2.2K-J | 2 | 10 |  | C |
|  | 26008115 | Carbon film resistor | R-25-22K-J | 1 | 10 |  | C |
|  | 26003318 | Carbon film resistor | R-25-220-J | 2 | 10 |  | C |
|  | 26006112 | Carbon film resistor | R-25-3.3K-J | 25 | 10 |  | C |
|  | 26009316 | Carbon film resistor | R-25-68K-J | 1 | 10 |  | C |
|  | 26007119 | Carbon film resistor | R-25-8.2K-J | 1 | 10 |  | C |
|  | 26004713 | Carbon film resistor | R-25-820-J | 2 | 10 |  | C |
|  | 26001714 | Carbon film resistor | R-25-47-J | 1 | 10 |  | C |
|  | 26007518 | Carbon film resistor | R-25-12K-J | 2 | 10 |  | C |
|  | 26009910 | Carbon film resistor | R-25-120K-J | 2 | 10 |  | C |
|  | 26010713 | Carbon film resistor | R-25-270K-J | 2 | 10 |  | C |
|  | 26006511 | Carbon film resistor | R-25-4.7K-J | 1 | 10 |  | C |
|  | 26005914 | Carbon film resistor | R-25-2.7K-J | 1 | 10 |  | C |
|  | 26005116 | Carbon film resistor | R-25-1.2K-J | 1 | 10 |  | C |
|  | 26004110 | Carbon film resistor | R-25-470-J | 1 | 10 |  | C |
|  | 26000912 | Carbon film resistor | R-25-22-J | 1 | 10 |  | C |
|  | 00028722 | Carbon film resistor | R-25-5K-J | 5 | 10 |  | C |
|  | 28080387 | Electrolytic capacitor | SMC50VB-2R2(M) | 1 | 10 |  | C |
|  | 28055064 | Electrolytic capacitor | SMC50VB-R1(M)-T | 3 | 10 |  | C |

Note: - New part
Q'ty - Quantity used per unit

*     - Minimum order/supply quantity

Rank A: Essential
B: Stock recommended
C: Others
X: No stock recommended

| Item | Code No． | Part Name | Specification | Q＇ty | ＊ | Unit Price J．F．Yen（ $¥$ ） （FOB：JAPAN） | R A N K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 4 | 28045051 | Electrolytic capacitor | 16RE10 | 1 | 10 |  | C |
|  | 00028720 | Electrolytic capacitor | 6．3RE2－470 | 4 | 10 |  | C |
|  | 28081014 | Electrolytic capacitor | SMC50VB－1MBP－T | 3 | 10 |  | C |
|  | 28056389 | Electrolytic capacitor | SMC16VB－10（M） | 7 | 10 |  | C |
|  | 28081111 | Electrolytic capacitor | SMC16VB－100（M）－T | 1 | 10 |  | C |
|  | 28081138 | Electrolytic capacitor | SMC16VB－33（M）－T | 1 | 10 |  | C |
|  | 28180055 | Ceramic capacitor | HE40SJYB221K | 8 | 10 |  | C |
|  | 28186191 | Ceramic capacitor | HE40SJSL220K | 1 | 10 |  | C |
|  | 28182040 | Ceramic capacitor | HE70SJYF103Z | 25 | 10 |  | C |
| क | 28182414 | Ceramic capacitor | RT－HE40TKSL－ $560 \mathrm{~K}-\mathrm{T}$ | 1 | 10 |  | C |
|  | 28183097 | Ceramic capacitor | HE40SJCH220J | 2 | 10 |  | C |
| \％ | 00028705 | Ceramic capacitor | HE11SJSL681K | 1 | 10 |  |  |
|  | 28186045 | Ceramic capacitor | HE40SJSL680K | 1 | 10 |  | C |
|  | 28203080 | TF capacitor | ECQ－V1H－104－JZ | 2 | 10 |  | C |
| 定 | 00028709 | TF capacitor | ECQ－B1H333KHW | 1 | 10 |  | C |
| \％ | 00028710 | TF capacitor | ECO－B1H562KHW | 2 | 10 |  | C |
| \％ | 43073320 | PCB－M5153－MA1M | M1658－1 | 1 |  |  | X |
|  |  | 2）MA2M PCB ASS＇Y |  |  |  |  |  |
| 它 | 20021144 | IC | $\mu \mathrm{PC} 1571 \mathrm{C}$ | 2 |  |  | A |
|  | 21003662 | MOS IC | TC4069 $\mu \mathrm{BP}$ | 3 |  |  | A |
|  | 21007692 | MOS IC | MN3209 | 3 |  |  | A |
|  | 21210013 | OP AMP | NJM4558DD | 3 |  |  | A |
|  | 28080298 | Electrolytic capacitor | SMC16VB－470（M） | 1 | 10 |  | C |
|  | 35003428 | Connector 9P | IL－G－9P－S3T2－E | 1 |  |  | $x$ |
| 的 | 35008177 | 6P connector M153A | IL－6P－10－M153 | 1 |  |  | $x$ |
|  | 38410661 | Low pass filter | LPF－M152－17K | 1 |  |  | B |
|  | 22201395 | Transistor | 2SC1740SO | 4 | 10 |  | B |
|  | 23013002 | Diode | DS－442 | 10 | 10 |  | C |
|  | 26007313 | Carbon film resistor | R－25－10K－J | 6 | 10 |  | C |
|  | 26007712 | Carbon film resistor | R－25－15K－J | 5 | 10 |  | C |
|  | 26007917 | Carbon film resistor | R－25－18K－J | 5 | 10 |  | C |
|  | 26008514 | Carbon film resistor | R－25－33K－J | 6 | 10 |  | C |
|  | 26008719 | Carbon film resistor | R－25－39K－J | 2 | 10 |  | C |
|  | 26009111 | Carbon film resistor | R－25－56K－J | 4 | 10 |  | C |
|  | 26004918 | Carbon film resistor | R－25－1K－J | 9 | 10 |  | C |
|  | 26010314 | Carbon film resistor | R－25－180K－J | 6 | 10 |  | C |
|  | 26005710 | Carbon film resistor | R－25－2．2K－J | 1 | 10 |  | C |
| Note：is－New part <br> Q＇ty－Quantity used per unit <br> ＊－Minimum order／supply quantity |  |  | Rank | A：Essential <br> B：Stock recommended <br> C：Others <br> X：No stock recommended |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | ． |  |  |  |
|  |  |  |  |  |  |  |


| Item | Code No. | Part Name | Specification | Q'ty | * | Unit Price J.F. Yen ( $¥$ ) (FOB: JAPAN) | $R$ $A$ N K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 26008115 | Carbon film resistor | R-25-22K-J | 15 | 10 |  | C |
|  | 26010519 | Carbon film resistor | R-25-220K-J | 3 | 10 |  | C |
|  | 26008310 | Carbon film resistor | R-25-27K-J | 5 | 10 |  | C |
|  | 26006112 | Carbon film resistor | R-25-3.3K-J | 2 | 10 |  | C |
|  | 26011116 | Carbon film resistor | R-25-390K-J | 1 | 10 |  | C |
|  | 26008913 | Carbon film resistor | R-25-47K.J | 6 | 10 |  | C |
|  | 26009316 | Carbon film resistor | R-25-68K-J | 3 | 10 |  | C |
|  | 26009910 | Carbon film resistor | R-25-120K-J | 1 | 10 |  | C |
|  | 26010110 | Carbon film resistor | R-25-150K-J | 9 | 10 |  | C |
|  | 26011515 | Carbon film resistor | R-25-560K-J | 3 | 10 |  | C |
|  | 26006511 | Carbon film resistor | R-25-4.7K-J | 3 | 10 |  | C |
|  | 26009511 | Carbon film resistor | R-25-82K-J | 1 | 10 |  | C |
|  | 26016398 | Carbon film resistor | R-25-6.8M-J | 1 | 10 |  | C |
|  | 28055013 | Electrolytic capacitor | SMC16VB-47(M)-T | 2 | 10 |  | C |
|  | 28049013 | Electrolytic capacitor | 50 RNBBP 1 | 6 | 10 |  | C |
|  | 28045051 | Electrolytic capacitor | 16RE10 | 1 | 10 |  | C |
|  | 28081014 | Electrolytic capacitor | SMC50VB-1MBP-T | 2 | 10 |  | C |
|  | 28080310 | Electrolytic capacitor | SMC50VB-1 (M) | 7 | 10 |  | C |
|  | 28081049 | Electrolytic capacitor | SMC50VB-3R3(M) | 4 | 10 |  | C |
|  | 28056389 | Electrolytic capacitor | SMC16VB-10(M) | 8 | 10 |  | C |
|  | 28056117 | Electrolytic capacitor | SMC25VB-10(M) | 6 | 10 |  | C |
|  | 28180110 | Ceramic capacitor | HE50SJYB102K | 3 | 10 |  | C |
|  | 28182040 | Ceramic capacitor | HE70SJYF103Z | 9 | 10 |  | C |
| * | 00028706 | Ceramic capacitor | HE60SJSL181K | 3 | 10 |  | C |
|  | 28190280 | Ceramic capacitor | HE60SJSL151K | 2 | 10 |  | C |
|  | 28183259 | Ceramic capacitor | HE11SJCH221J | 6 | 10 |  | C |
|  | 28186053 | Ceramic capacitor | HE50SJSL101K | 2 | 10 |  | C |
| \% | 00028711 | TF capacitor | ECQ-B1H102KHW | 3 | 10 |  | C |
| 4 | 00028708 | TF capacitor | ECQ-B1H103KHW | 1 | 10 |  | C |
| 公 | 00028712 | TF capacitor | ECQ-B1H222KHW | 1 | 10 |  | C |
| $\stackrel{\text { ar }}{ }$ | 00028713 | Mylar capacitor | ECQ-B1H822KHW | 3 | 10 |  | C |
| 尔 | 00028714 | TF capacitor | ECQ-B1H123KHW | 3 | 10 |  | C |
| क | 00028715 | TF capacitor | ECQ-B1H183KHW | 1 | 10 |  | C |
| \# | 00028716 | Mylar capacitor | ECQ-B1H182KHW | 2 | 10 |  | C |
| A | 43073310 | PCB-M5153-MA2M | M1659-1 | 1 | 10 |  | X |

Note: ~ - New part
Q'ty - Quantity used per unit

*     - Minimum order/supply quantity

Rank A: Essential
B : Stock recommended
C: Others
X: No stock recommended


Note: - New part
Q'ty - Quantity used per unit

*     - Minimum order/supply quantity

Rank A: Essential
B : Stock recommended
C: Others
X: No stock recommended

| Item | Code No． | Part Name | Specification | Q＇ty | ＊ | Unit Price J．F．Yen $(\neq)$ （FOB：JAPAN） | R A K K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| म | 37210481 | PC joiner M153G | PCJ－JPSS－12－200 | 1 |  |  | B |
| म | 37210490 | PC joiner M153M | PCJ－JPSS－18－200 | 1 |  |  | B |
| म | 37210503 | PC joiner M153L | PCH－JPSS－20－330 | 1 |  |  | B |
| 动 | 37210511 | PC joiner M153H | PCJ－JPSS－27－175 | 1 |  |  | B |
|  | 60020248 | Joiner holder G545 | P4260－1 | 2 |  |  | X |
|  | 26004918 | Carbon film resistor | R－25－1K－J | 9 | 10 |  | C |
|  | 28182040 | Ceramic capacitor | HE70SJYF103Z | 9 | 10 |  | C |
| ＊${ }^{\text {a }}$ | 43073250 | PCB－M5153－MA4M | M1671－1 | 1 |  |  | X |
|  |  | 5）CN1M PCB ASS＇Y |  |  |  |  |  |
| \％ | 34101710 | Push switch | KHC10902 | 46 | 10 |  | B |
| 尔 | 37210449 | PC joiner M153E | PCJ－UV－23－180 | 1 |  |  | B |
| 家 | 37210457 | PC joiner M153J | PCJJPSS－15－30 | 1 |  |  | B |
|  | 62302348 | Joiner holder E71 | E41620A－1 | 1 |  |  | X |
|  | 23013002 | Diode | DS－442 | 46 | 10 |  | C |
|  | 23209811 | LED | LN266RPT | 45 | 10 |  | B |
|  | 26003911 | Carbon film resistor | R－25－390－J | 31 | 10 |  | C |
| $\hat{\sim}$ | 43073270 | PCB－M5153－CN1M | M1660－1 | 1 |  |  | x |
|  |  | 6）CN2M PCB ASS＇Y |  |  |  |  |  |
|  | 21210013 | OP amp | NJM4558DD | 1 |  |  | A |
|  | 27709605 | Variable resistor | EWA－NF0X05B14 | 1 | 10 |  | B |
|  | 27709761 | Slide VR | EWA－NA1X05B54 | 1 |  |  | B |
| น | 34101701 | Push switch | KHC10902 | 36 | 10 |  | B |
| \％ | 35008142 | 4P connector M153 | IL－4P－40－M153 | 1 |  |  | X |
| 㐫 | 35008185 | 9P connector M153B | IL－9P－32－M153 | 1 |  |  | $x$ |
| \％ | 35008193 | 5P connector M153B | IL－5P－24－M153 | 1 |  |  | $x$ |
| 令 | 35008231 | 3P connector M153A | IL－3P－30－M153 | 1 |  |  | $x$ |
|  | 23013002 | Diode | DS－442 | 37 | 10 |  | C |
|  | 23209811 | LED | LN266RPT | 27 | 10 |  | B |
|  | 26007313 | Carbon film resistor | R－25－10K－J | 1 | 10 |  | C |
|  | 26007712 | Carbon film resistor | R－25－15K－J | 5 | 10 |  | C |
|  | 26007917 | Carbon film resistor | R－25－18K－J | 2 | 10 |  | C |
|  | 26003911 | Carbon film resistor | R－25－390－J | 14 | 10 |  | C |
|  | 26004918 | Carbon film resistor | R－25－1K－J | 2 | 10 |  | C |
|  | 26010110 | Carbon film resistor | R－25－150K－J | 1 | 10 |  | C |
|  | 28190280 | Ceramic capacitor | HE60SJSL151K | 1 | 10 |  | C |
| ［ 2 | 43073220 | PCB－M5153－CN2M | M1661－1 | 1 |  |  | X |

Note：मे－New part
Q＇ty－Quantity used per unit
＊－Minimum order／supply quantity

Rank A：Essential
B：Stock recommended
C：Others
X：No stock recommended


Note: is - New part
Q'ty - Quantity used per unit

*     - Minimum order/supply quantity

Rank A: Essential
B : Stock recommended
C: Others
X: No stock recommended


Note: ~ New part
Q'ty - Quantity used per unit

*     - Minimum order/supply quantity

Rank A: Essential
B : Stock recommended
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| Item | Code No. | Part Name | Specification | Q'ty | * | Unit Price J.F. Yen ( $¥$ ) (FOB: JAPAN) | $R$ $A$ $N$ K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 23104539 | Zener diode | RD5.6EL2 | 2 | 10 |  | B |
| 云 | 23105276 | Zener diode | RD8.2EL2 | 1 | 10 |  | B |
| म | 23107456 | Zener diode | RD6.2EL1 | 1 | 10 |  | B |
|  | 23301075 | Diode | S4VB10 | 1 | 10 |  | B |
|  | 26001315 | Carbon film resistor | R-25-33-J | 1 | 10 |  | C |
|  | 26002516 | Carbon film resistor | R-25-100-J | 2 | 10 |  | C |
|  | 26005116 | Carbon film resistor | R-25-1.2K-J | 1 | 10 |  | C |
|  | 26005311 | Carbon film resistor | R-25-1.5K-J | 1 | 10 |  | C |
|  | 26005515 | Carbon film resistor | R-25-1.8K-J | 1 | 10 |  | C |
|  | 26005710 | Carbon film resistor | R-25-2.2K-J | 1 | 10 |  | C |
|  | 26009715 | Carbon film resistor | R-25-100K-J | 1 | 10 |  | C |
|  | 26012911 | Carbon film resistor | R-25-10-J | 1 | 10 |  | C |
|  | 26204313 | Carbon film resistor | R-50X-560-J | 1 | 10 |  | C |
|  | 26302510 | Carbon film resistor | R-1W-100-J | 1 | 10 |  | C |
|  | 26313210 | Carbon film resistor | R-1W-0.47-J | 2 | 10 |  | C |
| \% 4 | 28045841 | Electrolytic capacitor | 16RE2-4700 | 1 | 10 |  | C |
| \% | 28045859 | Electrolytic capacitor | 35RE2-1000 | 2 | 10 |  | C |
| \% | 28056273 | Electrolytic capacitor | SMC6.3VB-470(M) | 3 | 10 |  | C |
|  | 28080271 | Electrolytic capacitor | SMC10VB-220(M) | 3 | 10 |  | C |
|  | 28080280 | Electrolytic capacitor | SMC25VB-220(M) | 1 | 10 |  | C |
|  | 28080298 | Electrolytic capacitor | SMC16VB-470(M) | 2 | 10 |  | C |
|  | 28080310 | Electrolytic capacitoe | SMC50VB-1 (M) | 1 | 10 |  | C |
|  | 35003355 | Pin ass'y 3P | IL-G-3P-S3T2-E | 1 | 10 |  | X |
| 4 | 35007610 | Pin ass'y 5P | IL-G-5P-S3T2-E | 1 | 10 |  | X |
|  | 35008215 | 9P connector M153C | IL-9P-70-M153 | 1 |  |  | X |
|  | 36402357 | Fuse clip | UF-0033\#01 | 6 | 10 |  | $x$ |
| क | 43073260 | PCB-M5153-PS2M | M2973-1 | 1 |  |  | x |
| $\stackrel{3}{4}$ | 69046380 | Heat sink 153 | M42191-1 | 1 |  |  | X |
| \% | 69046410 | Heat sink | M42301-1 | 1 |  |  | X |
|  |  | 11) IF PCB ASS ${ }^{+}$ |  |  |  |  |  |
|  | 35106481 | P.C.B. connector | $\begin{aligned} & \text { PS30PE-S4LT1 } 1 \\ & \text { PN1** } \end{aligned}$ | 1 |  |  | $x$ |
| 的 | 37208761 | PC joiner | SMCD-26-140 | 1 |  |  | B |
|  | 43072960 | PCB-M4150-IF | M31576-1 | 1 |  |  | X |
|  | 60020248 | Joiner holder G545 | P4260-1 | 1 |  |  | X |

Note: $\Rightarrow$ - New part
Q'ty - Quantity used per unit

*     - Minimum order/supply quantity

Rank A: Essential
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C: Others
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Note: मे - New part
Q'ty - Quantity used per unit

*     - Minimum order/supply quantity

Rank A: Essential
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| Item | Code No． | Part Name | Specification | Q＇ty | ＊ | Unit Price J．F．Yen（ $¥$ ） （FOB：JAPAN） | R A N K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 4 令 | 39045210 | Key D | M31568－1 | 5 |  |  | C |
| 5 파 | 69045220 | Key G | M31569－1 | 5 |  |  | C |
| 6 म 7 | 69045230 | Key S | M31570－1 | 1 |  |  | C |
| 7 站 | 69045240 | Black key | M31571－1 | 25 |  |  | C |
| 8 | 69046350 | Key stopper 61A | M42126－1 | 1 |  |  | C |
| 9 | 69046360 | Upper case stopper | M42130－1 | 1 |  |  | C |
| 10 安 | 69016161 | S felt 61C | M4925A－1 | 1 |  |  | X |
| 11\％ | 69045280 | Rubber switch G | M31553－1 | 4 |  |  | B |
| 12\％ | 69045290 | Rubber switch H | M31554－1 | 1 |  |  | B |
| 13 | 69045301 | KB guide C | M31630A－1 | 4 |  |  | X |
| 14\％ | 69045311 | KB guide D | M31631A－1 | 1 |  |  | $x$ |
| 15安 | 00028827 | $K B$ chassis | M2992－1 | 1 |  |  | X |
|  |  | 17）WHEEL ASS＇Y |  |  |  |  |  |
| 16 | 27706843 | Variable resistor | VM10W520A－50KB | 2 |  |  | B |
| 17 \％ | 35008151 | 6P connector M153B | IL－6P－95－M153 | 1 |  |  | X |
| 18荿 | 69040420 | Bender spring | M41737－1 | 1 | 50 |  | B |
| 19 号 | 69040430 | Felting seal 71A | M41812－1 | 2 | 10 |  | X |
| 20＊ | 69046110 | Bender knob 153 | M31620－1 | 2 | 10 |  | C |
| 21 云 | 69046120 | Bender chassis 153 | M42128－1 | 2 |  |  | $x$ |
| 22云 | 69115250 | Bender chassis B | M41946－1 | 2 |  |  | $x$ |
|  |  | 18）RAM PACK CASE | SS＇Y |  |  |  |  |
| 23尔 | 69045950 | RAM pack compartment upper case subass＇y | M31651＊1 | 1 |  |  | $x$ |
| 24 | 69046090 | RAM pack compartment lower case | M31621－1 | 1 |  |  | X |
| 25管 | 69046100 | RAM pack house holder | M42129－1 | 1 |  |  | $x$ |
| 26的 | 00028822 | RAM pack cover | M31489－1 | 1 |  |  | C |
| 27 动 | 69115320 | Shaft | M41948－1 | 1 |  |  | $x$ |
| 28出 | 69115330 | Spring | M41947－1 | 1 | 50 |  | C |
|  | 00028824 | PE washer | M41951A－1 | 2 | 50 |  | C |
|  |  | 19）BATTERY BOX SUB | $A S S ' Y$ |  |  |  |  |
| 30 约 | 35008258 | 2P connector M153A | IL－2P－40－M153 | 1 |  |  | $x$ |
| 31 | 60006091 | Battery spring G67 | A43656－1 | 1 | 50 |  | C |
| 32 | 63249297 | Battery spring C－G164 | A43733－1 | 1 | 50 |  | C |

Note：\＆－New part
Q＇ty－Quantity used per unit
＊－Minimum order／supply quantity

Rank A：Essential
B ：Stock recommended
C：Others
X：No stock recommended

| Item | Code No． | Part Name | Specification | Q＇ty | ＊ | Unit Price J．F．Yen（ $¥$ ） （FOB：JAPAN） | R A $N$ $K$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 33 | 63281560 | Battery spring G49 | A44683－1 | 1 | 50 |  | C |
| 34 | 63452238 | Battery spring A－G55 | A42606A－1 | 1 | 50 |  | C |
| 35 今 | 00028826 | Battery box | M1303－3 | 1 |  |  | C |
|  |  | 20）SIDE BOARD SUBASS＇Y |  |  |  |  |  |
| 36 | 69040260 | Rhythm button | M4498－11 | 1 |  |  | C |
|  | 69045820 | Side board subass＇y（Left） | M31654＊1 | 1 |  |  | C |
| 38ヶ | 69045660 | Side board subass＇y（Right） | M31652＊1 | 1 |  |  | C |
|  |  | 21）KEY TOP |  |  |  |  |  |
| 39 动 | 69048640 | Key top／djd | M31623－6 | 1 |  |  | C |
| 40 | 69048650 | Key top／d $d_{0}$ | M31623－7 | 1 |  |  | C |
| 41\％ | 69048660 | Key top／REST | M31623－8 | 1 |  |  | C |
| 42出 | 69048670 | Key top／－ | M31623－9 | 1 |  |  | C |
| 43出 | 69048680 | Key top／ | M31623－10 | 1 |  |  | C |
| 44出 | 69048690 | Key top／$\vdash^{3} \square$ | M31623－11 | 1 |  |  | C |
| 45号 | 69048700 | Key top／ $\mid$ \｜： $\mid$ | M31623－12 | 1 |  |  | C |
| 46出 | 69048710 | Key top $/\\|\bullet \Pi:\\|^{\text {® }}$ | M31623－13 | 1 |  |  | C |
| 47分 | 69048720 | Key top／A | M31623－14 | 2 |  |  | C |
| 48令 | 69048730 | Key top／B | M31623－15 | 2 |  |  | C |
| 49 \％ | 69048740 | Key top／C | M31623－16 | 2 |  |  | C |
| 50 江 | 69048750 | Key top／D | M31623－17 | 2 |  |  | C |
| 51 m | 69048760 | Key top／ 1 | M31623－18 | 1 |  |  | C |
| 52 하 | 69048770 | Key top／ 2 | M31623－19 | 1 |  |  | C |
| 53号 | 69048780 | Key top／ 3 | M31623－20 | 1 |  |  | C |
| 54尔 | 69048790 | Key top／ 4 | M31623－21 | 1 |  |  | C |
| 55. | 69048800 | Key top／ 5 | M31623－22 | 1 |  |  | C |
| 56 场 | 69048810 | Key top／ 6 | M31623－23 | 1 |  |  | C |
| 57的 | 69048820 | Key top／ 7 | M31623－24 | 1 |  |  | C |
| 58出 | 69048830 | Key top／ 8 | M31623－25 | 1 |  |  | C |
| 59 的 | 69048840 | Key top／Wave form | M31623－26 | 2 |  |  | C |
| 60的 | 69048850 | Key top／ENV | M31623－27 | 6 |  |  | C |
| 61 的 | 69048860 | Key top／Key follow | M31623－28 | 4 |  |  | C |
| 62安 | 69048870 | Key top／Porta－Mento | M31623－29 | 1 |  |  | C |
| 63家 | 69048880 | Key top／Glide | M31623－30 | 1 |  |  | C |
| 64 家 | 69048890 | Key top／Detune | M31623－31 | 1 |  |  | C |
| 65曻 | 69048900 | Key top／Key transpose | M31624－7 | 1 |  |  | C |

Note：मे－New part
Q＇ty－Quantity used per unit
＊－Minimum order／supply quantity

Rank A：Essential
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| Item | Code No． | Part Name | Specification | Q＇ty | ＊ | Unit Price J．F．Yen（ $¥$ ） （FOB：JAPAN） | R A N K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 66吘 | 69048910 | Key top／Normal | M31624－8 | 1 |  |  | C |
| 67\％ | 69048920 | Key top／Tone mix | M31624－9 | 1 |  |  | C |
| 68贸 | 69048930 | Key top／Key split | M31624－10 | 1 |  |  | C |
| 69部 | 69048940 | Key top／Solo | M31624－11 | 1 |  |  | C |
| 70\％ | 69048950 | Key top／MIDI | M31624－12 | 1 |  |  | C |
| 71 留 | 69048960 | Key top／V（Value／Save） | M31624－13 | 1 |  |  | C |
| 72 站 | 69048970 | Key top／ $\boldsymbol{\Delta}$（Value／Load） | M31624－14 | 1 |  |  | C |
| 73立 | 69048980 | Key top／＜（Consor／No） | M31624－15 | 1 |  |  | C |
| 74 $\%$ | 69048990 | Key top／（Consor／Yes） | M31624－16 | 1 |  |  | C |
| 75 出 | 69049000 | Key top／－Down | M31624－17 | 1 |  |  | C |
| 76\％ | 69049010 | Key top／© UP | M31624－18 | 1 |  |  | C |
| 77 立 | 69049020 | Key top／Sustain | M31624－19 | 1 |  |  | C |
| 78 玄 | 69049030 | Key top／End | M31624－20 | 1 |  |  | C |
| 79动 | 69049040 | Key top／MT | M31624－21 | 1 |  |  | C |
| 80 的 | 69049050 | Key top／Cartridge | M31624－22 | 1 |  |  | C |
| 81 的 | 69049060 | Key top／Porta－Mento | M31624－23 | 1 |  |  | C |
| 82 的 | 69049070 | Key top／Glide | M31624－24 | 1 |  |  | C |
| 83云 | 69049080 | Key top／Bend range | M31624－25 | 1 |  |  | C |
| 84的 | 69049090 | Key top／Modulation depth | M31624－26 | 1 |  |  | C |
| 85 m | 69049100 | Key top／Ring | M31624－27 | 1 |  |  | C |
| 86 的 | 69049110 | Key top／Noise | M31624－28 | 1 |  |  | C |
| 87 的 | 69049120 | Key top／Delete | M31624－29 | 1 |  |  | C |
| 88动 | 69049130 | Key top／VDown | M31624－30 | 1 |  |  | C |
| 89 的 | 69049140 | Key top／ $\mathbf{\Delta U p}$ | M31624－31 | 1 |  |  | C |
| 90 的 | 69049150 | Key top／Repeat | M31624－32 | 1 |  |  | C |
| 91 矿 | 69049160 | Key top／Real time | M31624－33 | 1 |  |  | C |
| 92完 | 69049170 | Key top／© Manual | M31624－34 | 1 |  |  | C |
| 93 䏣 | 69049180 | Key top／Reset | M31624－35 | 1 |  |  | C |
| 94碞 | 69049190 | Key top／＜R Rev | M31624－36 | 1 |  |  | C |
| 95 | 69049200 | Key top $/>$ FWD | M31624－37 | 1 |  |  | C |
| 96 令 | 69049210 | Key top／Play | M31624－38 | 1 |  |  | C |
| 97 珱 | 69049220 | Key top／－Stop | M31624－39 | 1 |  |  | C |
| 98站 | 69049230 | Key top／Compare／Recall | M31624－40 | 1 |  |  | C |
| 99安 | 69049240 | Key top／Track check | M31624－41 | 1 |  |  | C |
| 100 吹 | 69049250 | Key top／Write | M31624－42 | 1 |  |  | C |
| 101＊ | 69049260 | Key top／O Record | M31624－43 | 1 |  |  | C |
| 102 会 | 69049270 | Key top／Master tune | M31624－44 | 1 |  |  | C |
| 103 会 | 69049280 | Key top／Sequencer | M31624－45 | 1 |  |  | C |
| Note：合－New part <br> Q＇ty－Quantity used per unit <br> ＊－Minimum order／supply quantity |  |  |  | A： |  |  |  |
|  |  |  |  | $\begin{aligned} & \mathrm{B}: \\ & \mathrm{C}: \\ & \mathrm{X}: \end{aligned}$ |  | ommended <br> recommended |  |


| Item | Code No． | Part Name | Specification | Q＇ty | ＊ | Unit Price J．F．Yen（ $¥$ ） （FOB：JAPAN） | R A N K |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 104너 | 69049290 | Key top／Line select | M31624－46 | 1 |  |  | C |
| 105 | 69049300 | Key top／Vibrato | M31624－47 | 1 |  |  | C |
| 106＊ | 69049310 | Key top／Octave | M31624－48 | 1 |  |  | C |
| 107ヶ | 69049320 | Key top／Initialize | M31624－49 | 1 |  |  | C |
|  |  | 22）UPPER／LOWER CASE |  |  |  |  |  |
| 108； | 69045730 | Upper case subass＇y | M31670＊ 1 | 1 |  |  | c |
| 109 㣍 | 69045740 | Upper panel subass＇y （with key top set） | M1692＊ 1 | 1 |  |  | C |
| 110 ${ }^{\text {ct }}$ | 69026250 | Blind plate（for slide volume） | M41215－1 | 2 | （10） |  | c |
| 111住 | 69046140 | DIN jack holder 153 | M31619－1 | 1 |  |  | C |
| 112絡 | 69046420 | UL cover | M42302－1 | 1 |  |  | C |
| 113 | 69045670 | Lower case subass＇y | M21015＊1 | 1 |  |  | C |
|  |  | 23）OTHERS |  |  |  |  |  |
| 114 | 69014240 | Battery cover | M3615－2 | 1 |  |  | C |
| 115＊ | 69016470 | Transformer holder | M4887－1 | 2 |  |  | X |
| 116 | 69040050 | Power switch knob | M41093－3 | 1 |  |  | C |
| ［ | 69046150 | Case stopper rubber | M42190－1 | 1 | 10 |  | C |
| 117 | 69046160 | VR knob 153 | M31622－1 | 2 | 10 |  | C |
| 4 | 69202270 | Clip | CS－5 | 1 | 10 |  | C |
| $\stackrel{\rightharpoonup}{*}$ | 69046430 | Dust cover | M31736－1 | 1 |  |  | C |
|  | 37009491 | Plug cord set | 6．3MPP－L300－H－9 | 1 |  |  | C |

Note：$\hat{\text { b }}$－New part
Q＇ty－Quantity used per unit
＊－Minimum order／supply quantity

Rank
A：Essential
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C：Others
X：No stock recommended





[^0]:    $\mathrm{G} 2=\mathrm{G} 2 \mathrm{~A}+\mathrm{G} 2 \mathrm{~B}$
    $H=$ high level, $L=$ low level, $X=$ irrelevant

